

Angel_CY

UMA Schematics Document

IVY Bridge

Intel PCH

WWW.AITECH1.RU

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

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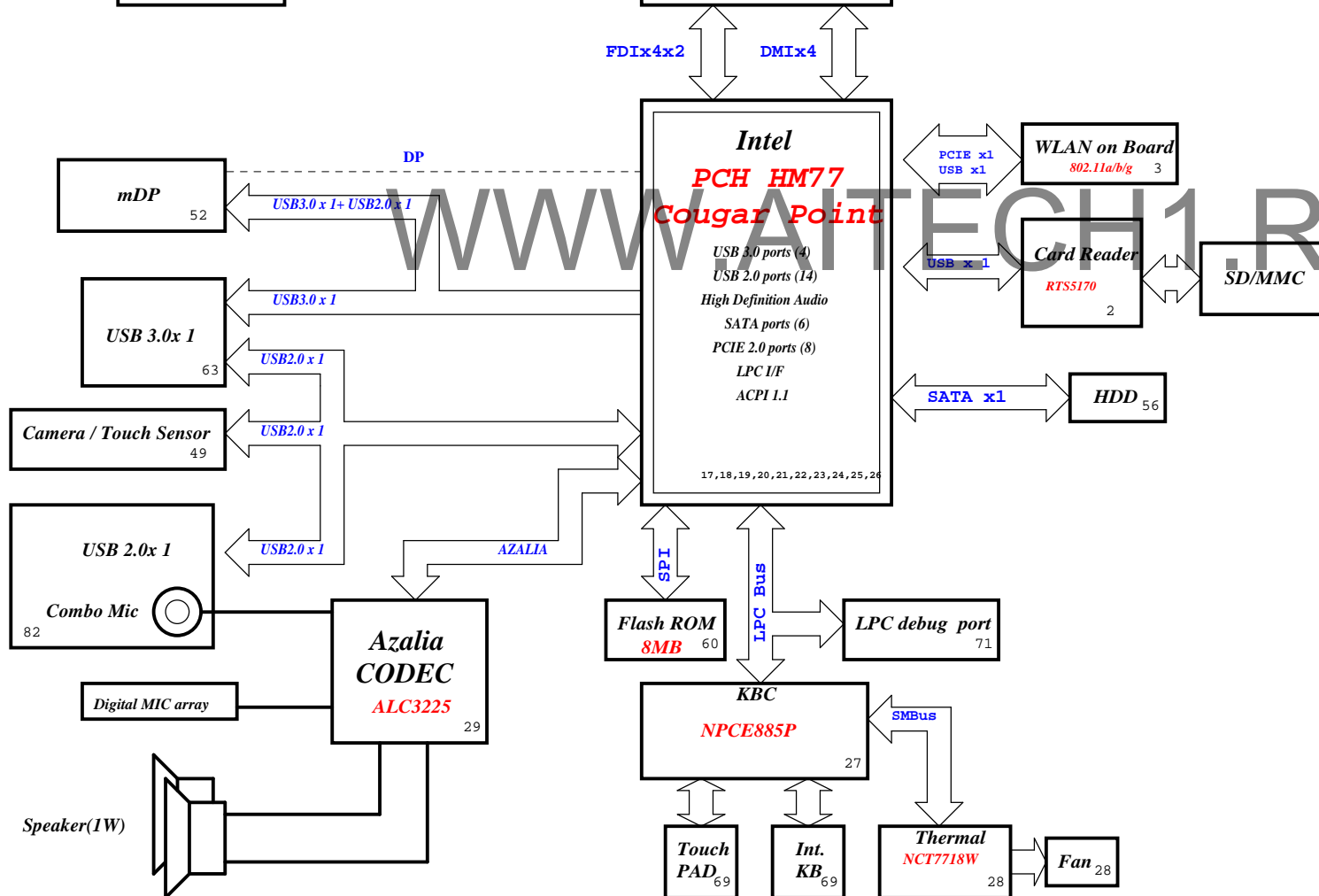
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Cover Page			
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Revision : 12313-1

The diagram illustrates the system architecture centered around an **Intel CPU** (IVY-Bridge, FSB: 1066 MHz). The CPU is connected to four components:

- DDR3L-SO DIMM** (15 pins): Connected via **DDRIII 1066/1333 Channel B**.
- Panel** (49 pins): Connected via **eDP**.
- RAM x 16** (1 pins): Four modules connected via **DDRIII 1066/1333 Channel A**.



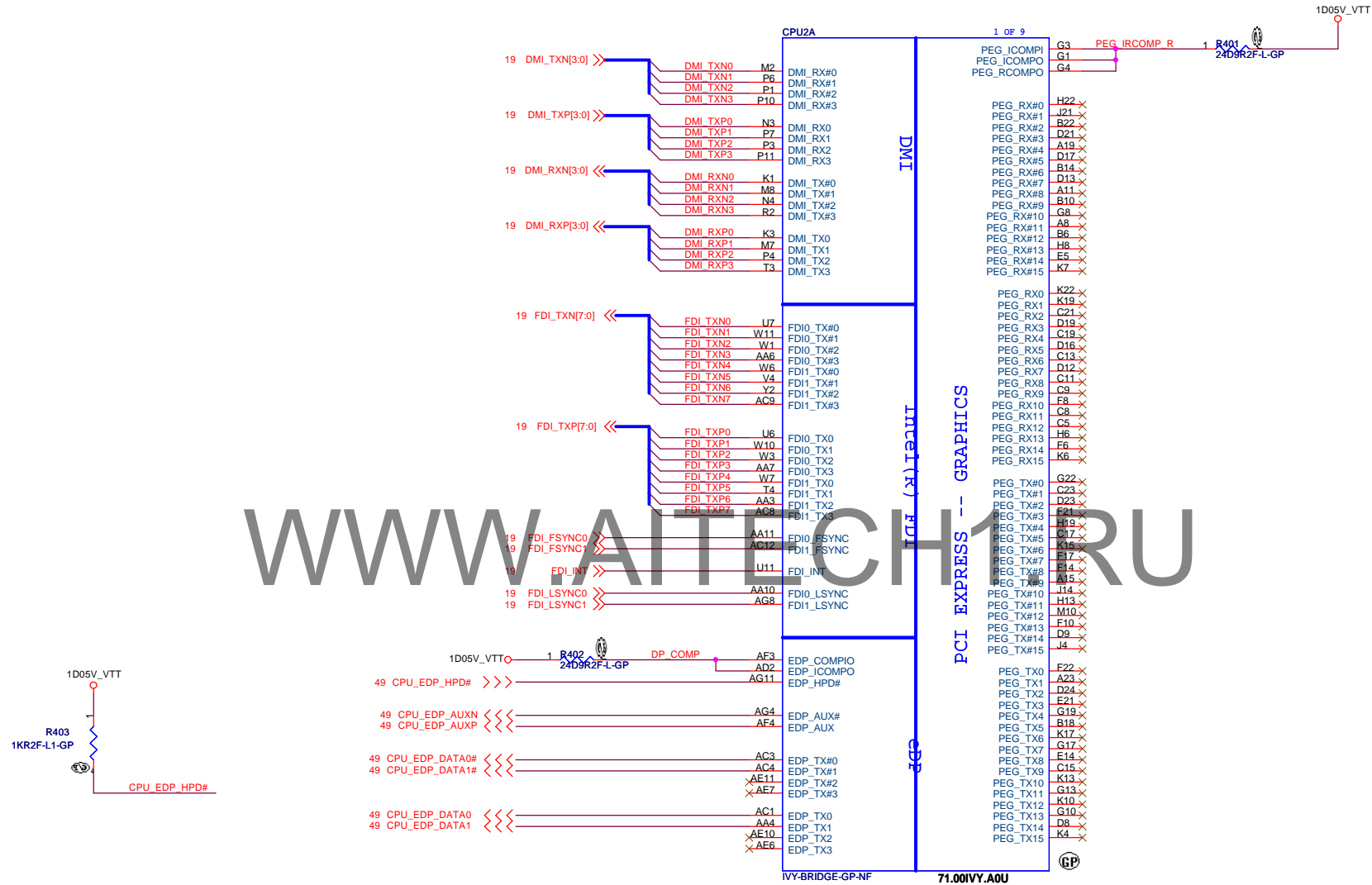
SYSTEM DC/DC		40
BQ24727		
INPUTS	OUTPUTS	
DCBATOUT	BT+	
SYSTEM DC/DC		41
TPS51225		
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5	
CPU DC/DC		42~44
TPS51640		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE VCC_GFXCORE	
SYSTEM DC/DC		45
TPS51363		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_VTT	
SYSTEM DC/DC		46
RT8207		
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3	
SYSTEM DC/DC		47
SYW232		
INPUTS	OUTPUTS	
3D3V_S0	1D8V_S0	
SYSTEM LOD		47
S-1339D		
INPUTS	OUTPUTS	
1D8V_S0	1D5V_S0	
SYSTEM DC/DC		48
SY8037		
INPUTS	OUTPUTS	
5V_S5	0D85V_S0	
PCB LAYER		
L1:Top	L5:Signal	
L2:VCC	L6:Signal	
L3:Signal	L7:GND	
L4:GND	L8:Bottom	

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Title			
Block Diagram			
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SSID = CPU

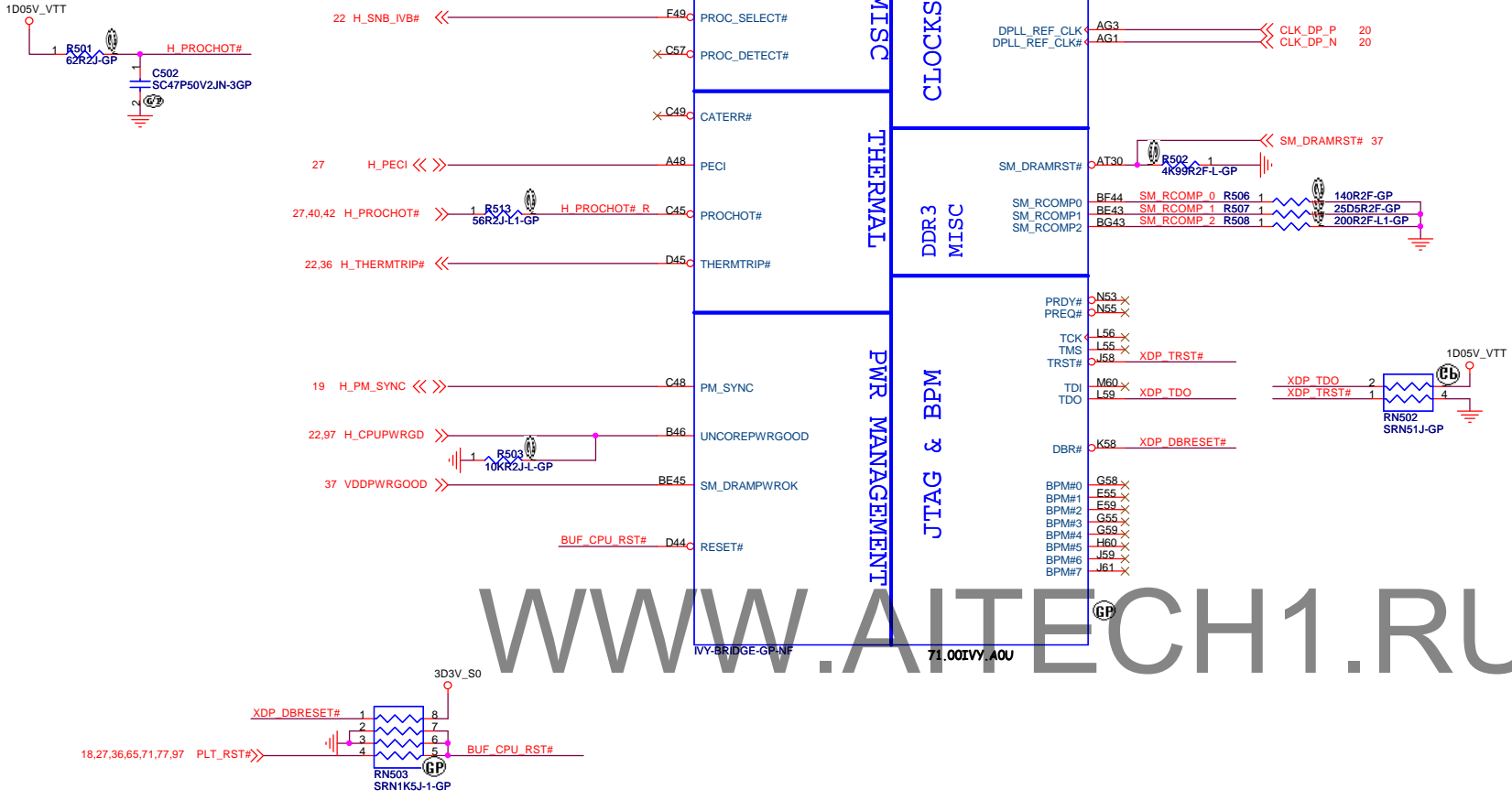


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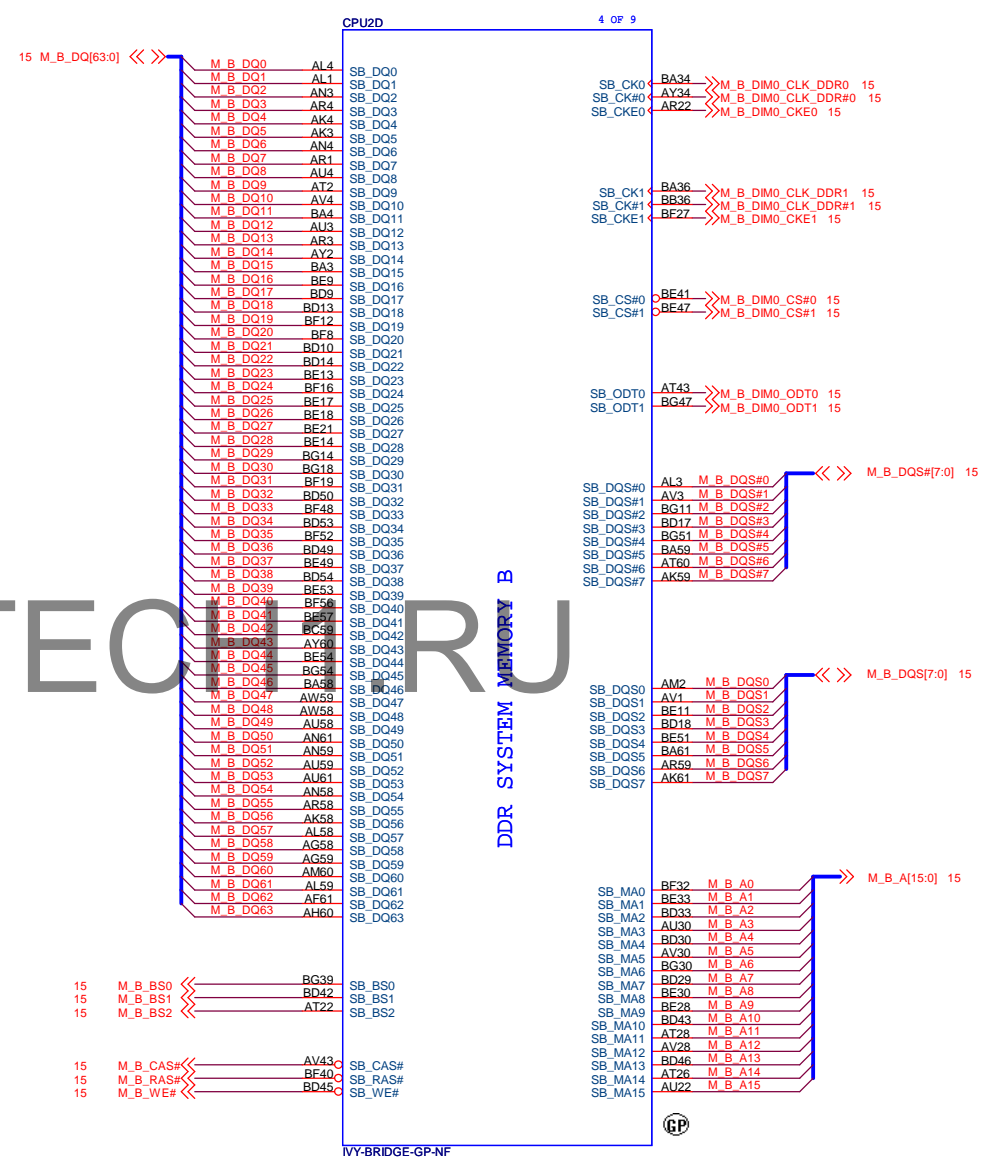
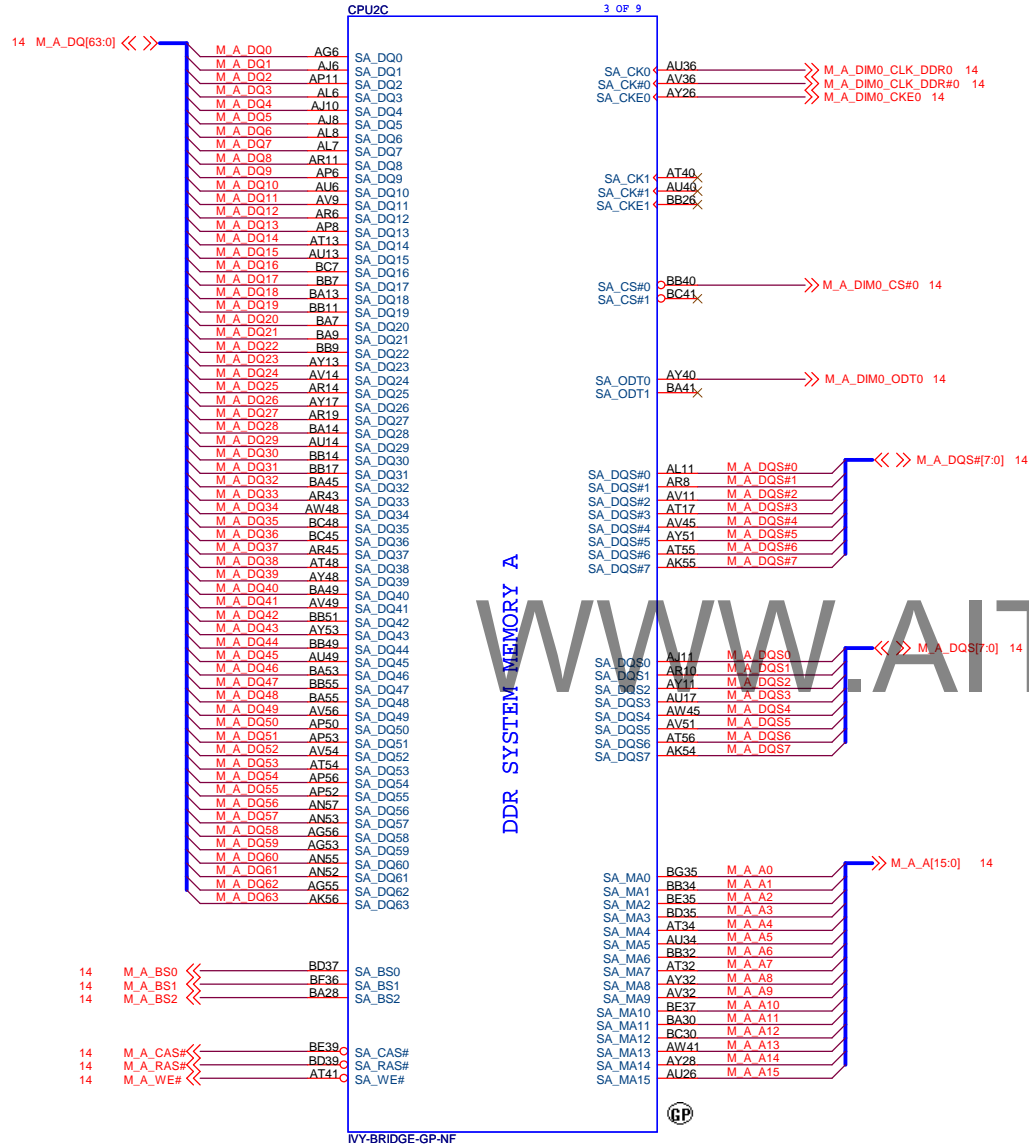
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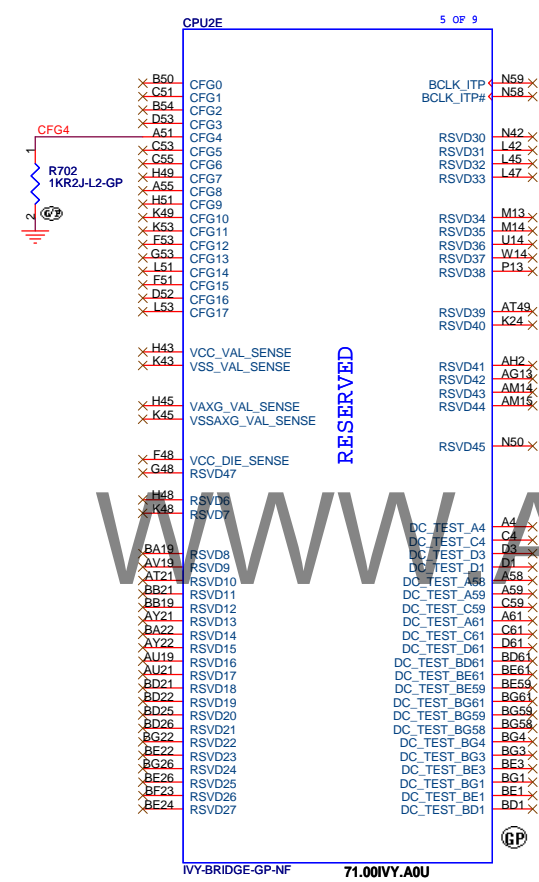


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Title CPU (DDR)	
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SSID = CPU



Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed	0
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort No connect for disable 0: Enabled - An external Display Port device is connected to the Embedded Display Port Pull-down to GND through a 1KΩ ± 5% resistor to enable port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	00
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

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Title

CPU (RESERVED)

Size

Document Number

Rev

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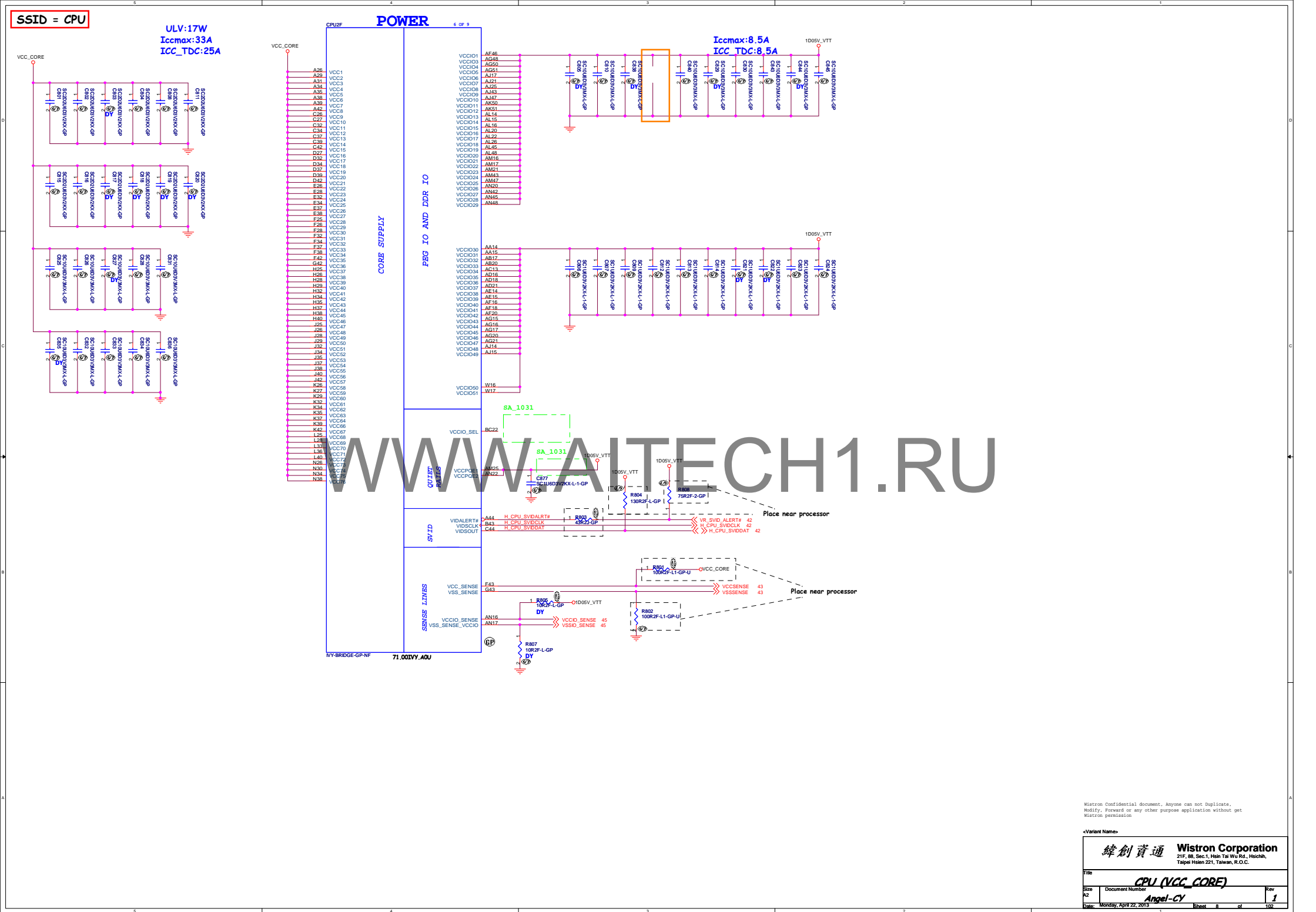
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ULV:17W
Iccmax:33A
ICC_TDC:25A



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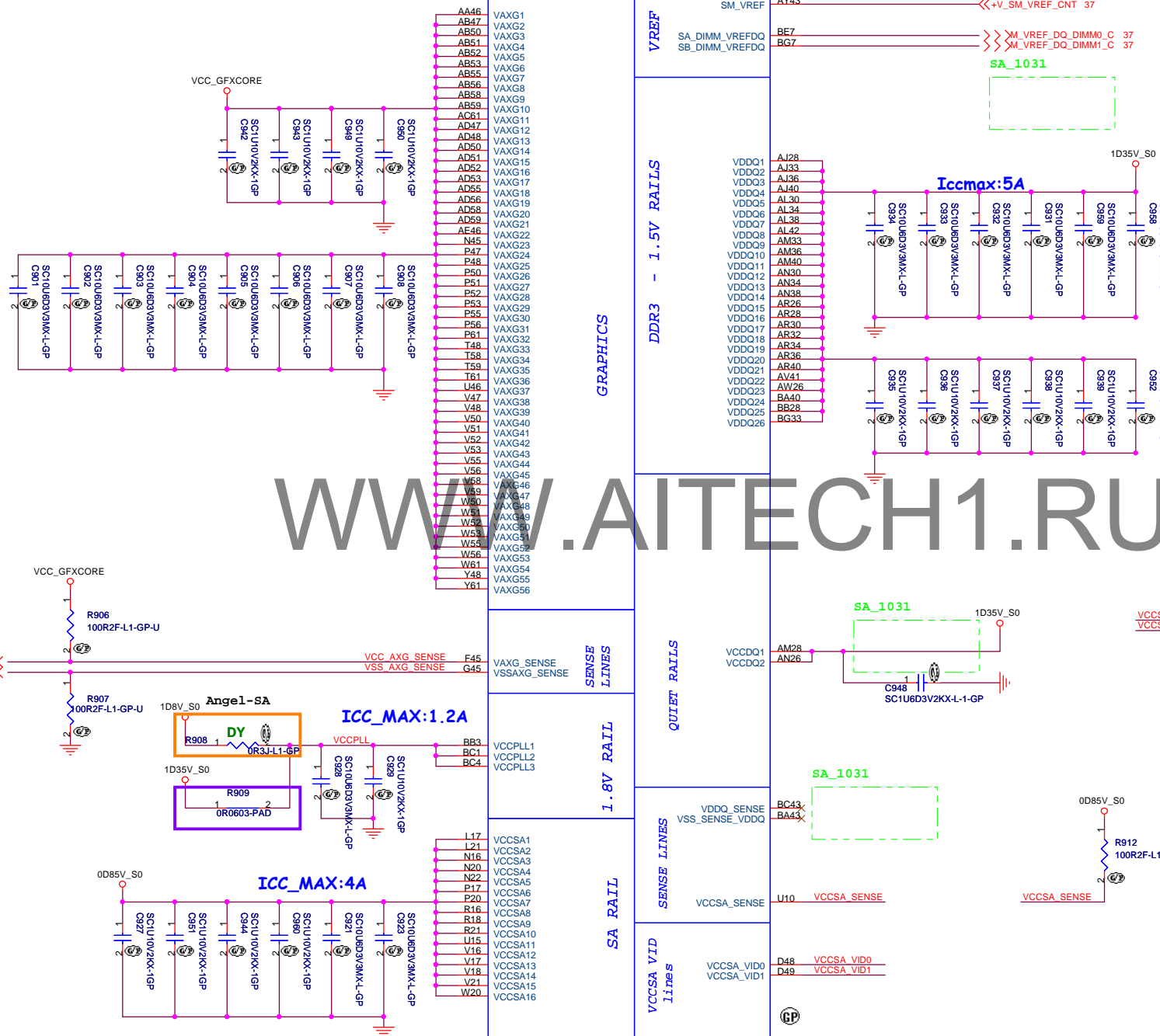
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Title			
CPU (VCC_CORE)			
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Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

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Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.



VID0	VID1	VCCSA ULV
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

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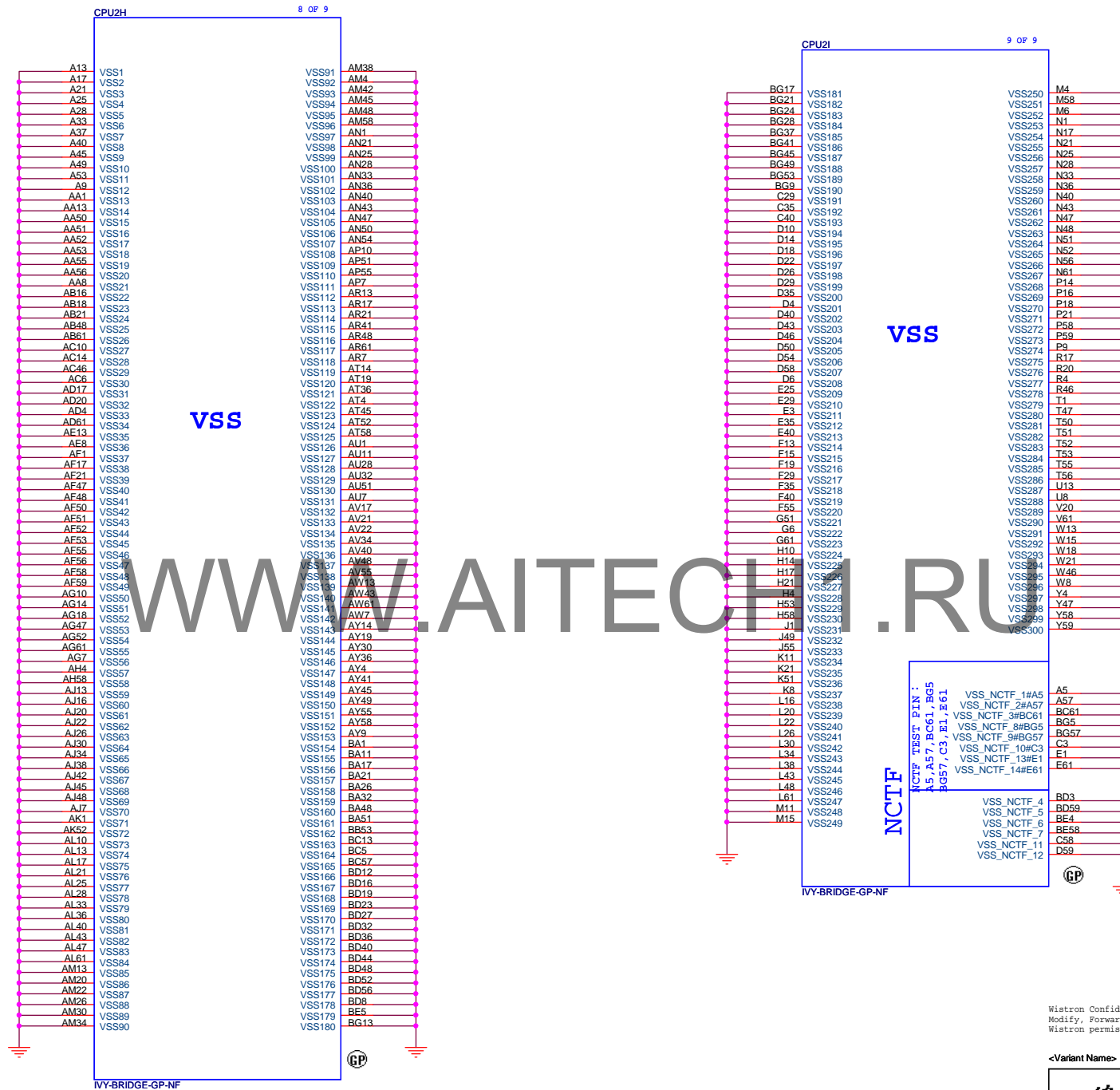
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Title	<i>CPU (VCC_GFXCORE)</i>
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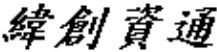
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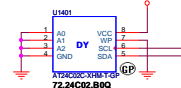
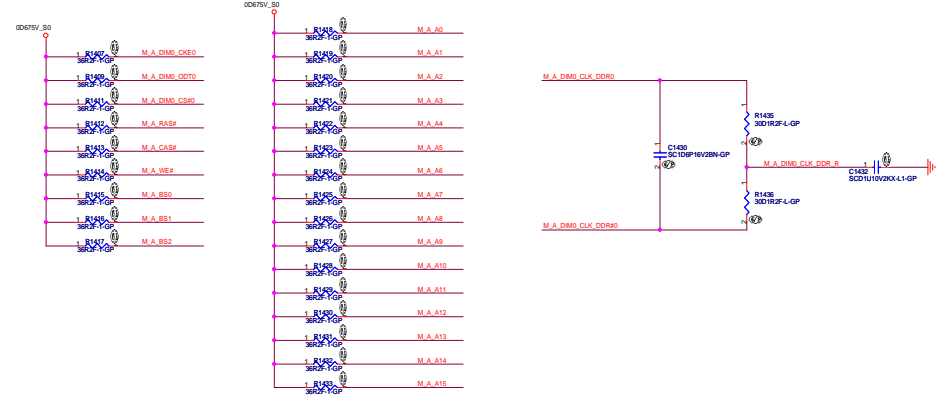
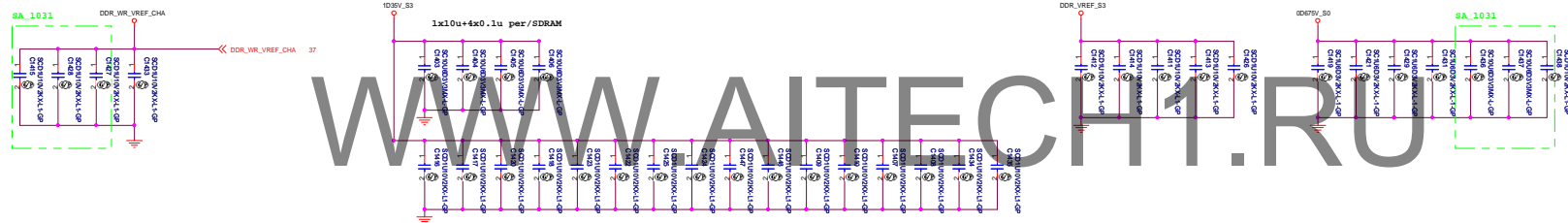
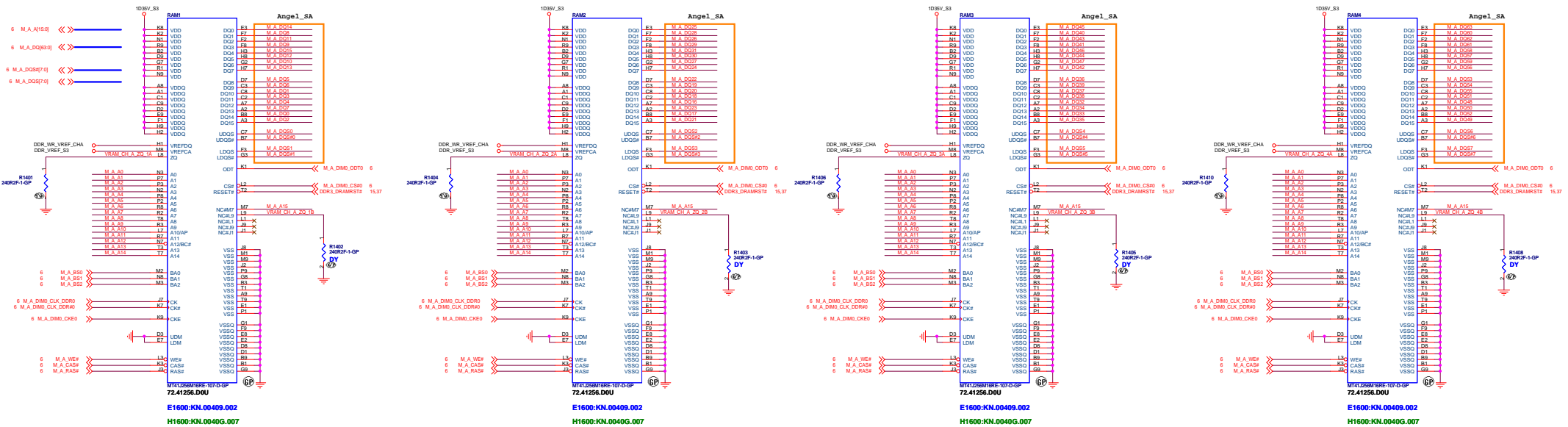
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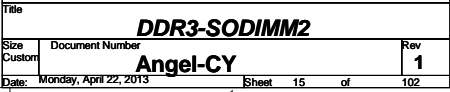
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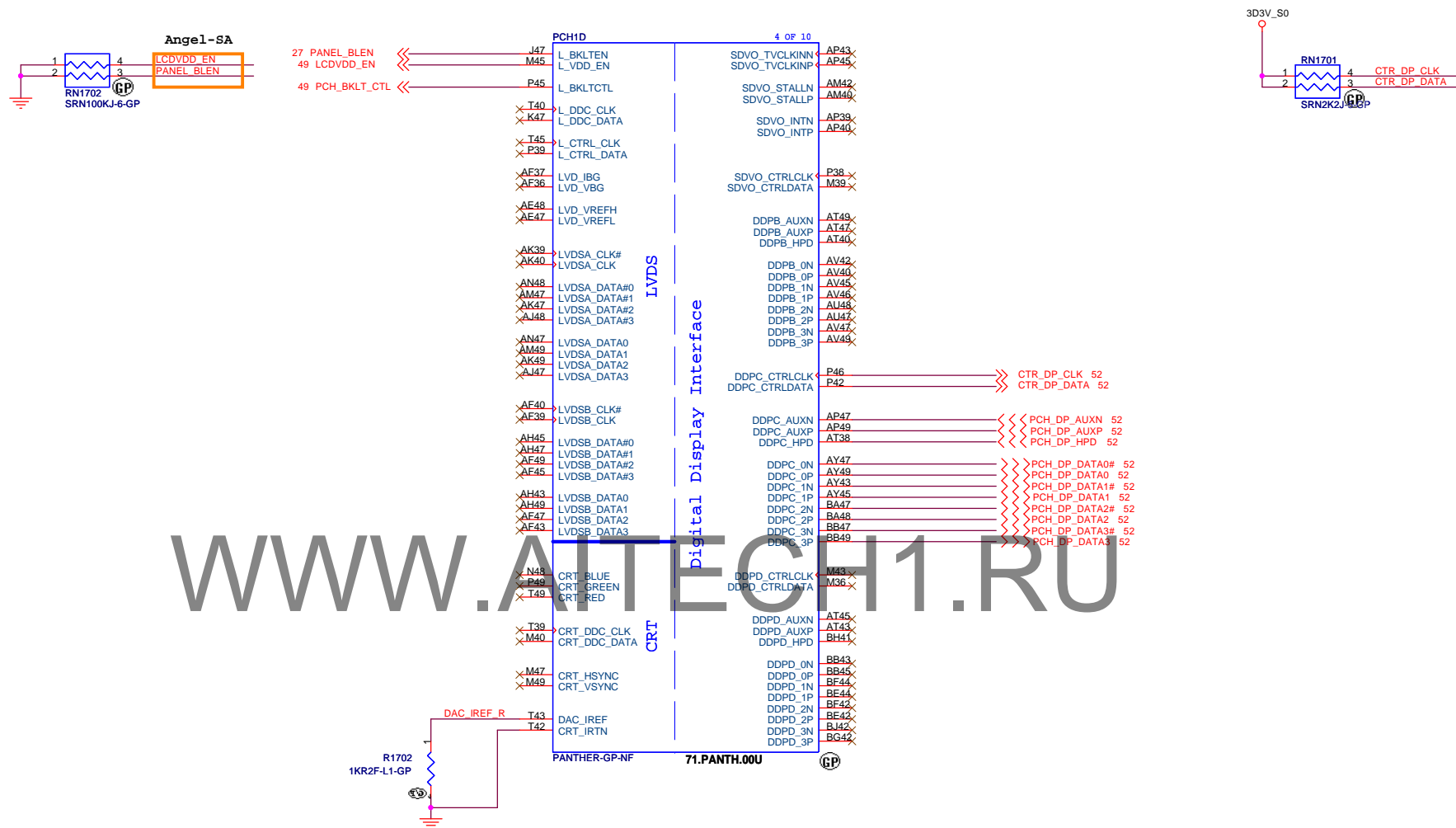
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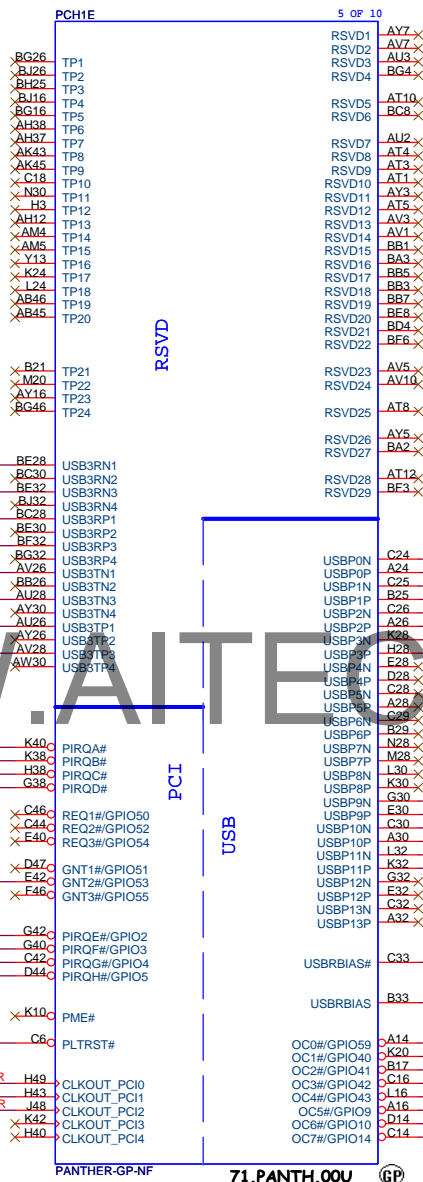
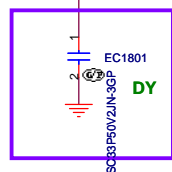
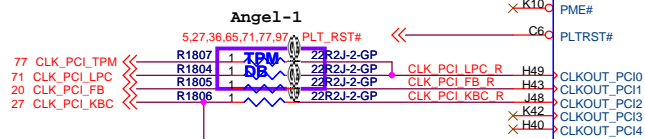
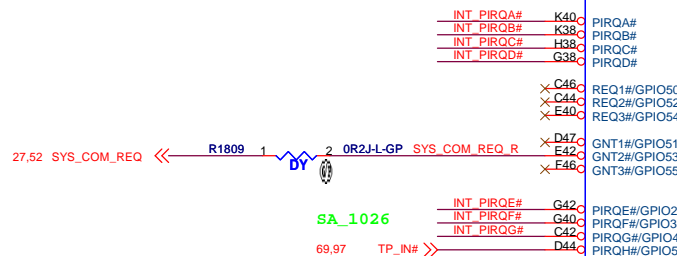
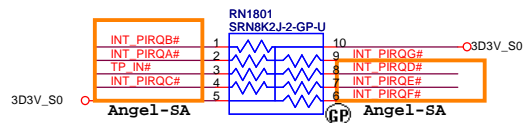


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Title PCH (LVDS/CRT/DDI)		
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SSID = PCH



USB Table

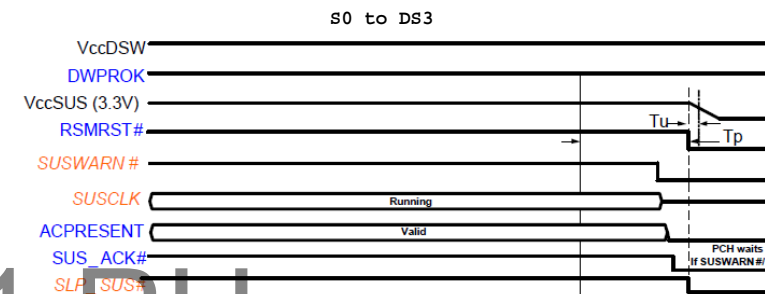
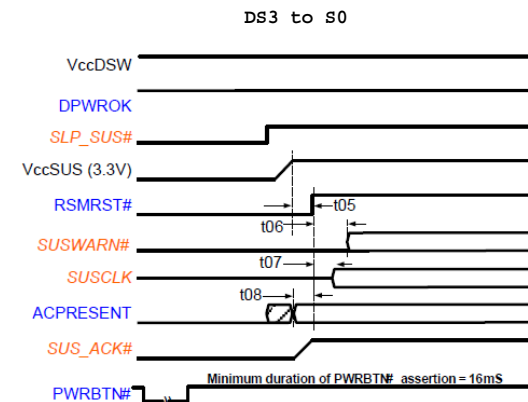
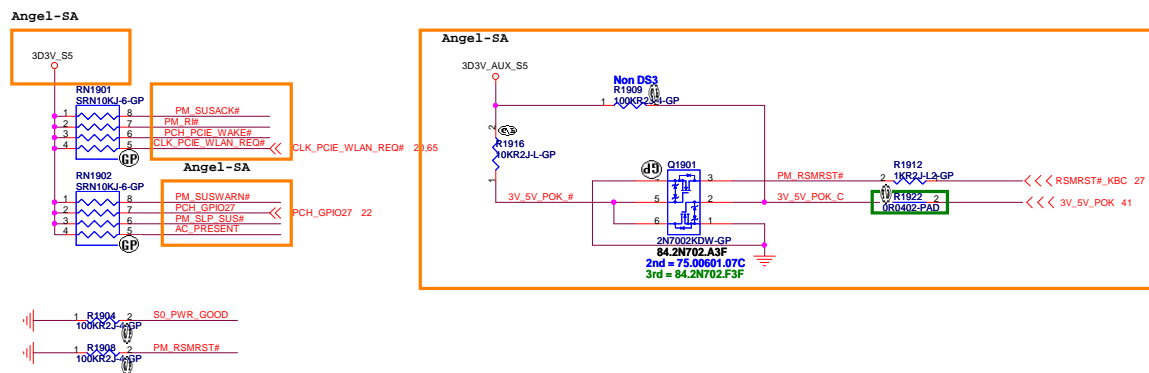
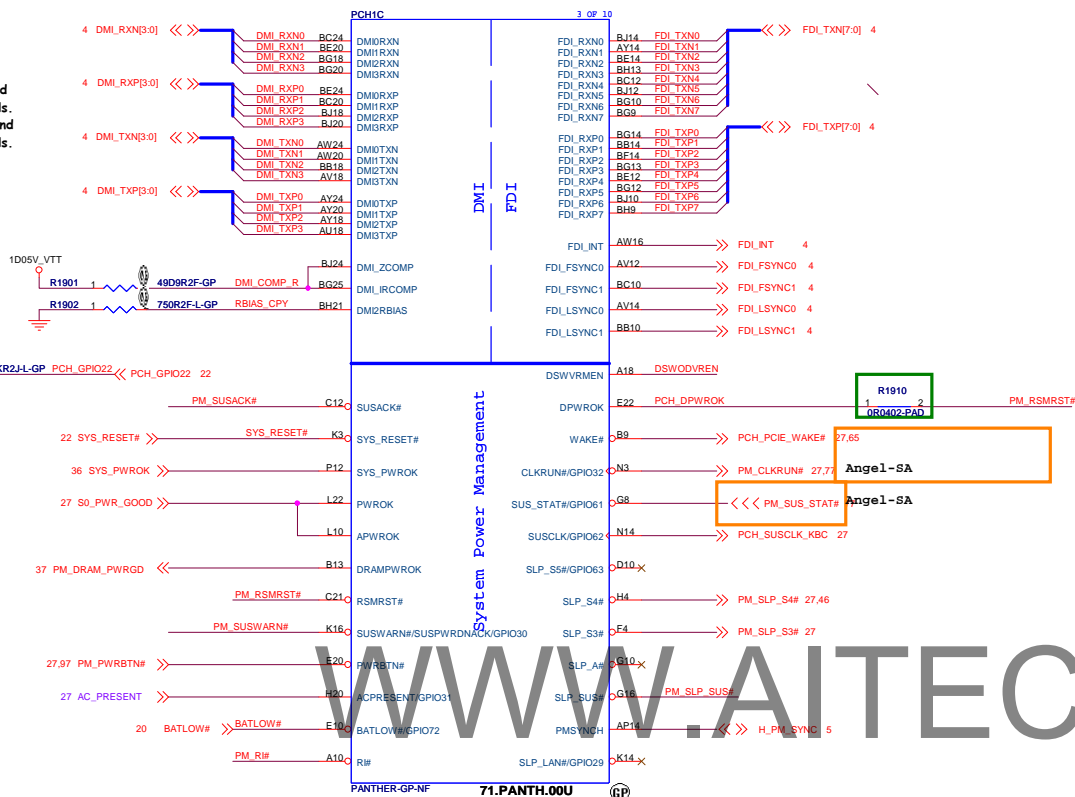
Pair	Device
0	USB3.0 Ext. port 1
1	TOUCH PANEL
2	mDP
3	CCD
4	NC
5	NC
6	X
7	X
8	NC
9	USB2.0 Ext. port 1
10	Card Reader
11	Mini Card1 (BT)
12	NC

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Title PCH (PCI/USB/NVRAM)		
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Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

The diagram shows a circuit connection for the DSWODVREN pin. A red line indicates the connection from the DSWODVREN pin to R1917, which is connected to the 330KR2F1-GP component. The RTC_AUX pin is also shown, connected to a red line.

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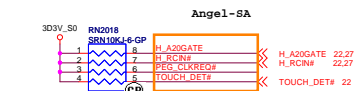
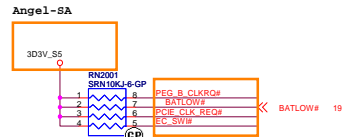
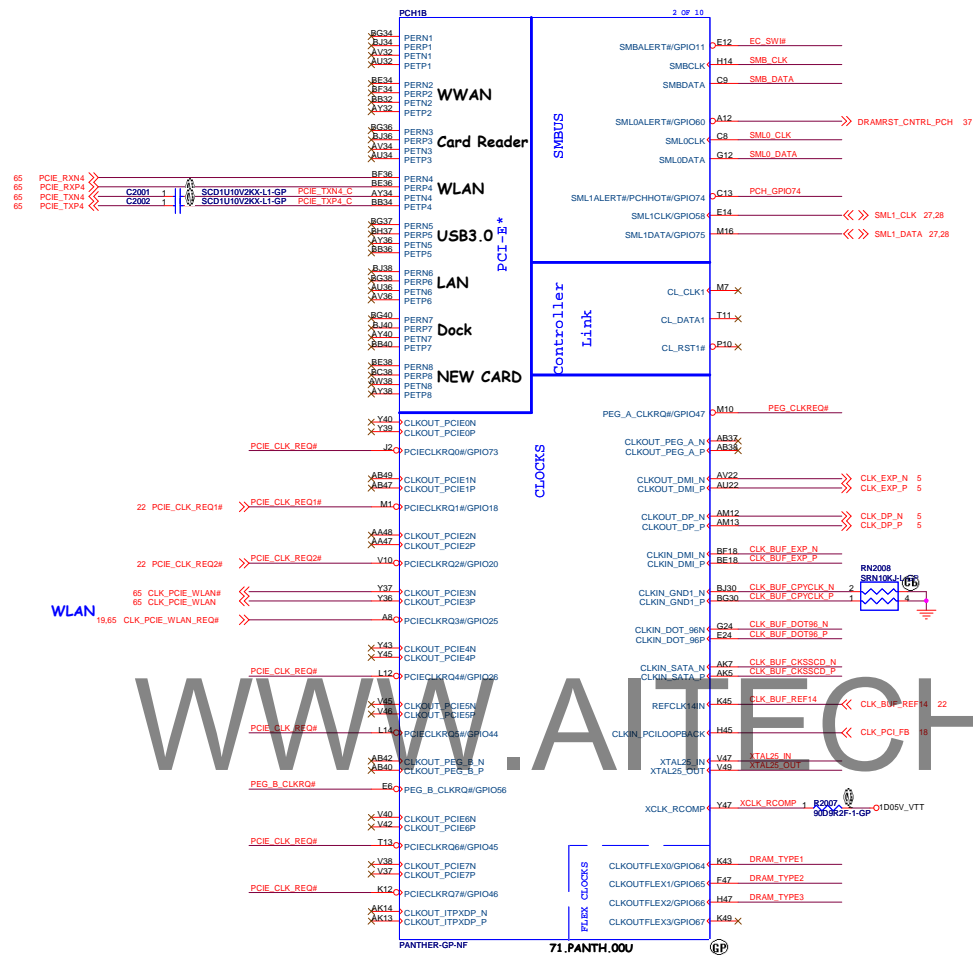
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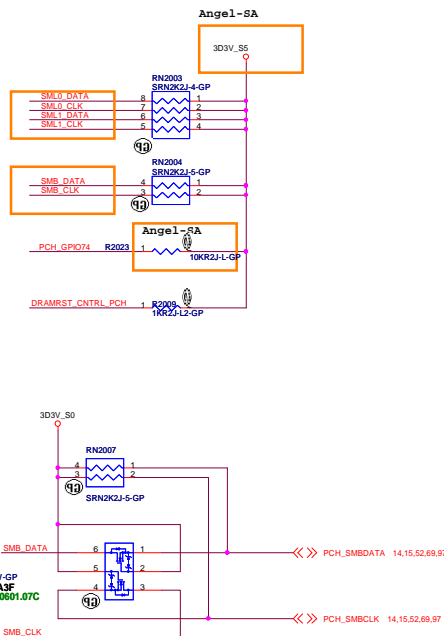
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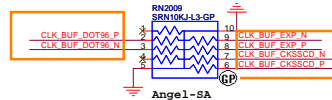
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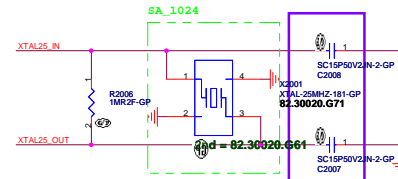
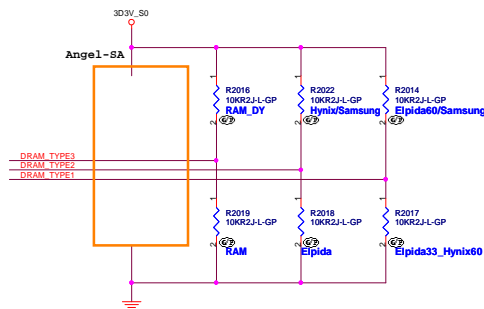
PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only



UMA_DIS#:D6PU_PSNT#
UMA: 1 1
DIS: 0 1
SG(PX): 0 0
Optimus(Muxless): 1 0



GPIO66 DRAM_Type3	GPIO65 DRAM_Type2	GPIO64 DRAM_Type1	Status
0	0	0	ELPIDA_KM.4GB09.003 ELPIDA DDR3L 1333 4Gb ED/4216EBBG-D1-F
0	0	1	ELPIDA_KN.00409.002 ELPIDA DDR3L 1600 4Gb ED/4216EBBG-GNL-F
0	1	0	Hynix_KN.0040G.007 HYNIX DDR3L 1600 4Gb H5TC4G63AFR-PBA LF+HF 256*16 29nm

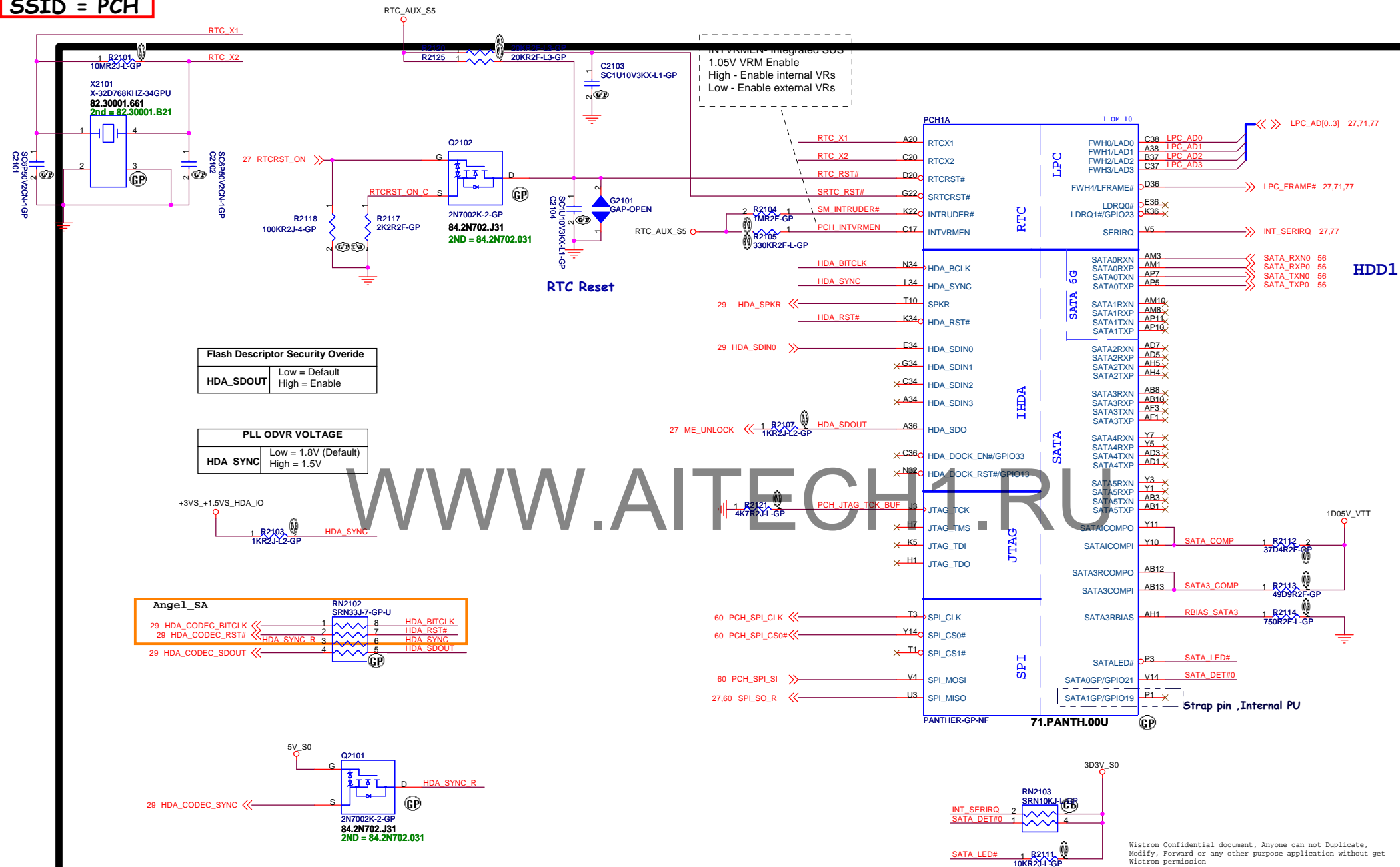


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Title PCH (PCI-E/SMBUS/CLOCK/CL)		
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SSID = PCH



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices(Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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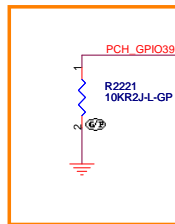
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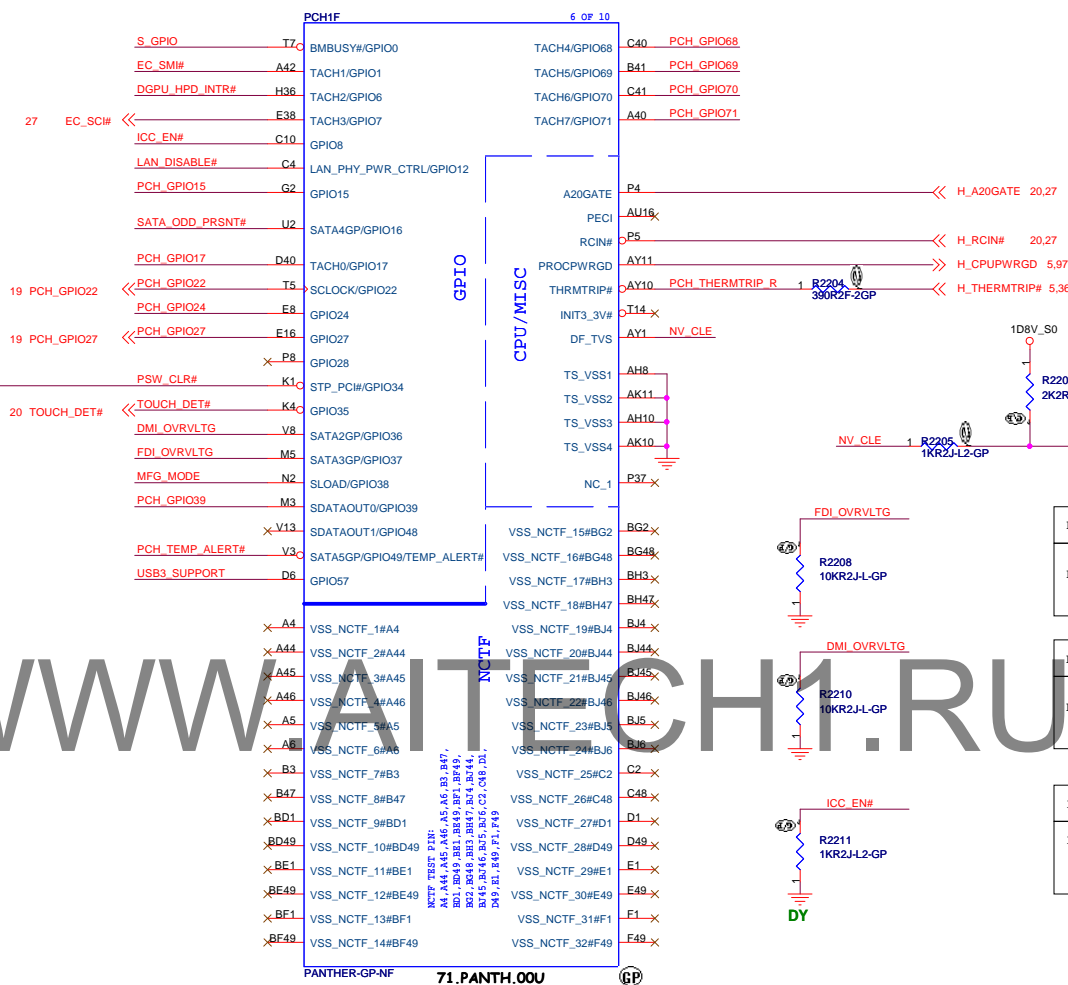
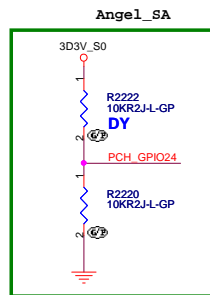
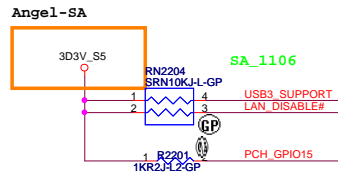
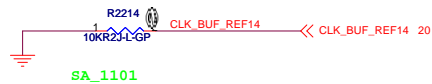
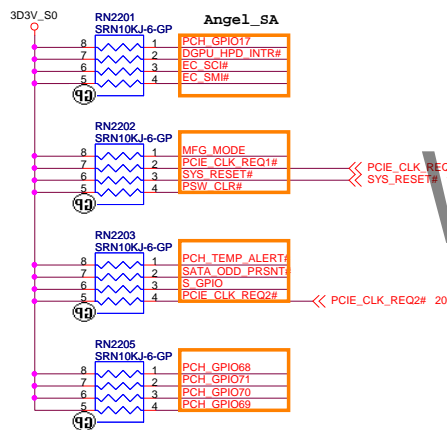
Title	PCH (SPI/RTC/LPC/SATA/IHDA)
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SSID = PCH



Pass Word Clear



FDI TERMINATION VOLTAGE OVERRIDE(Reserved)	
FDI_OVRVLTG (GPIO37)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE(Reserved)	
DMI_OVRVLTG (GPIO36)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable(Reserved)	
ICC_EN# (GPIO8)	HIGH- DISABLED [DEFAULT]
	LOW - ENABLED

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Title PCH (GPIO/CPU)	
Size Custom	Document Number Angel-CY
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SSID = PCH

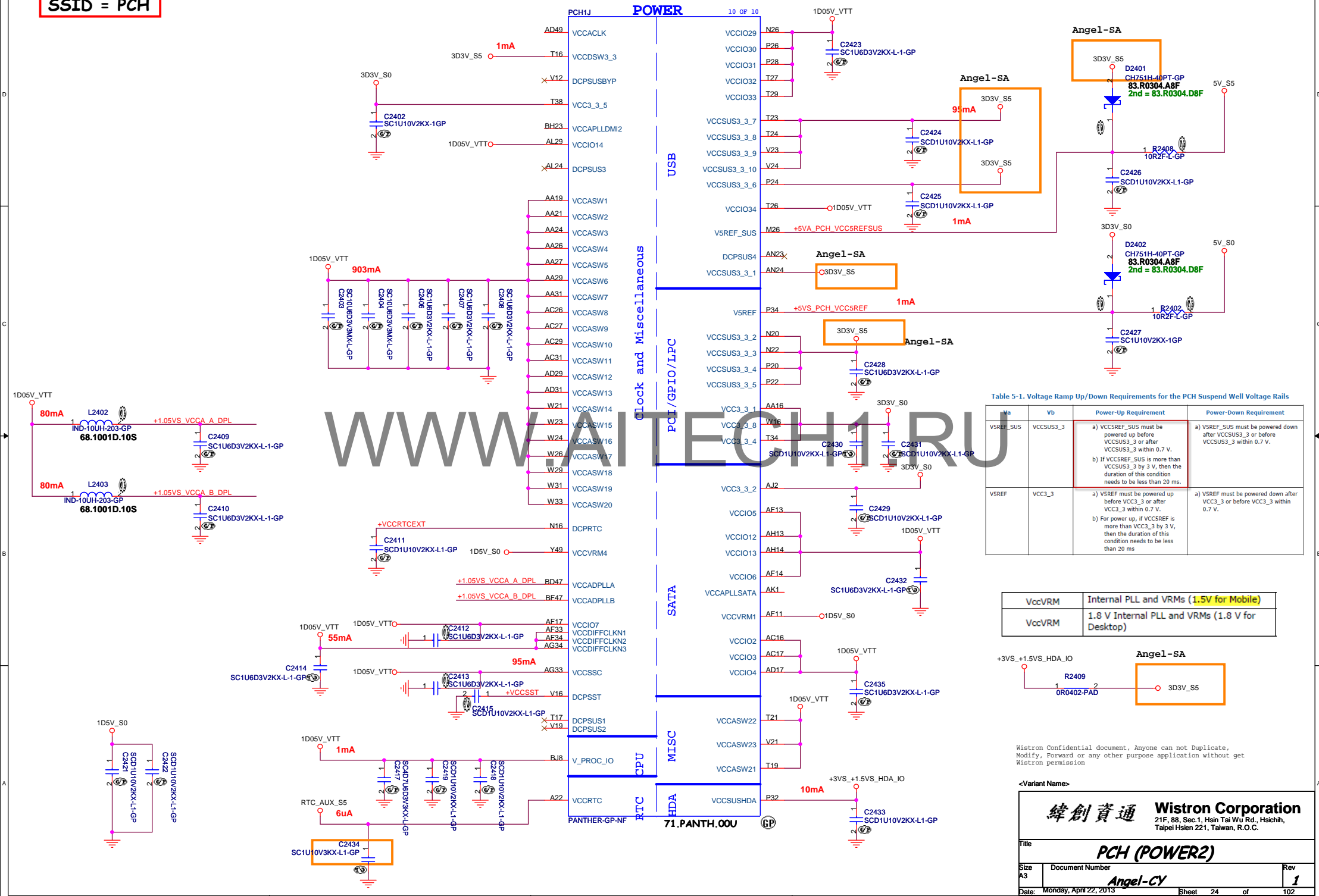
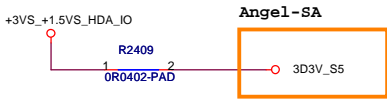


Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	<p>a) VCCSREF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V.</p> <p>b) If VCCSREF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.</p>	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	<p>a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V.</p> <p>b) For power up, if VCCSREF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms</p>	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)



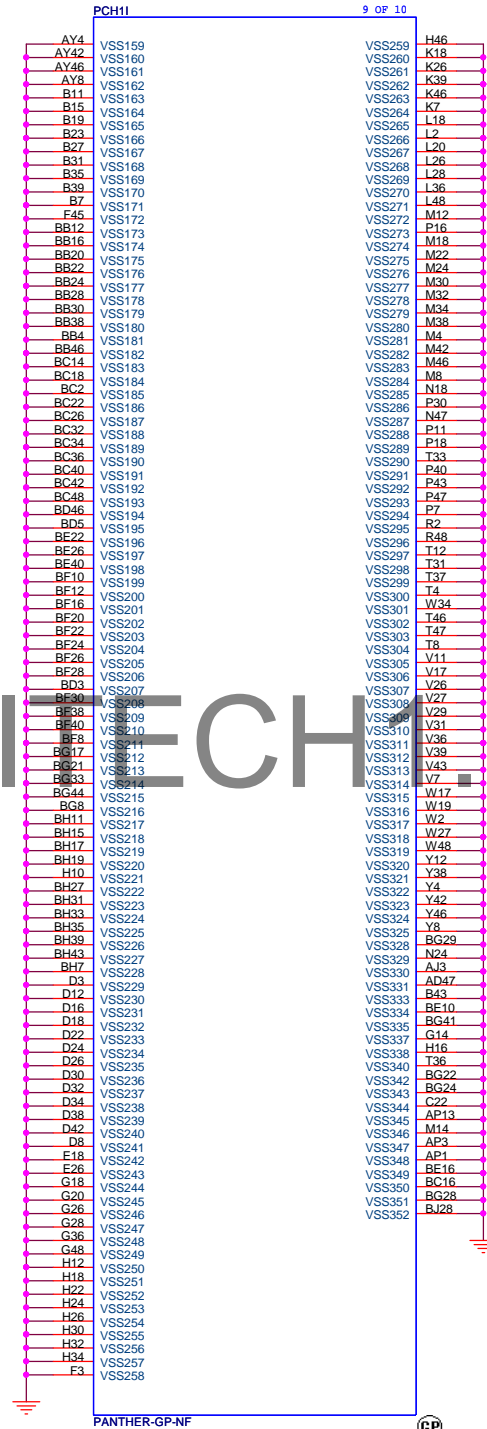
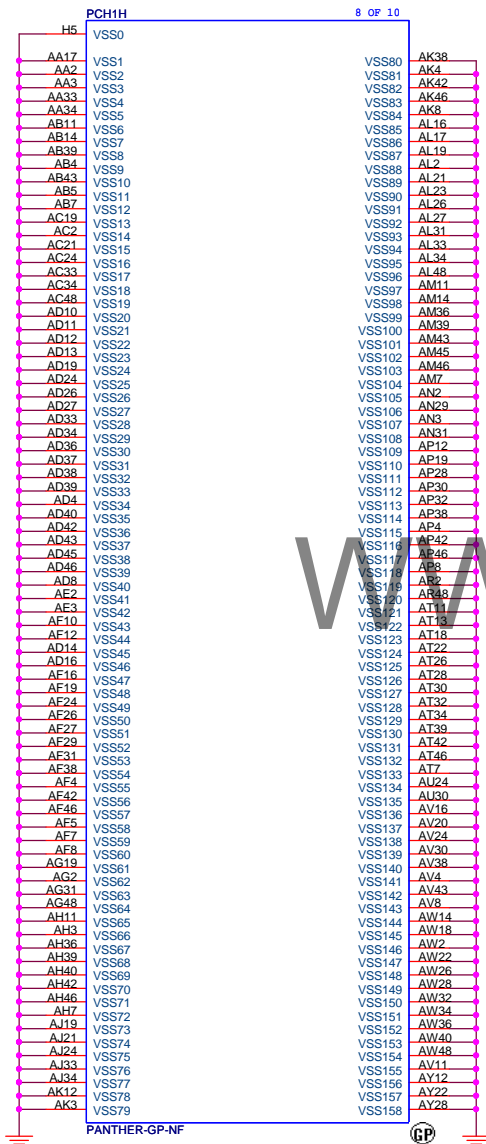
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Title				PCH (POWER2)			
Size A3		Document Number				Rev	
		Angel-CY				1	
Date:		Monday, April 22, 2013		Sheet 24 of		102	

SSID = PCH



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Title PCH (VSS)

Size A3 Document Number Angel-CY Rev 1

Date: Monday, April 22, 2013 Sheet 25 of 102

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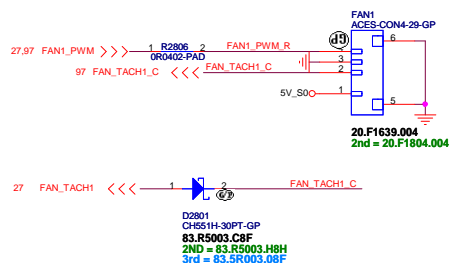
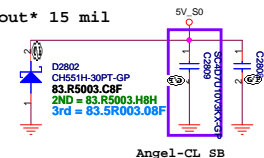
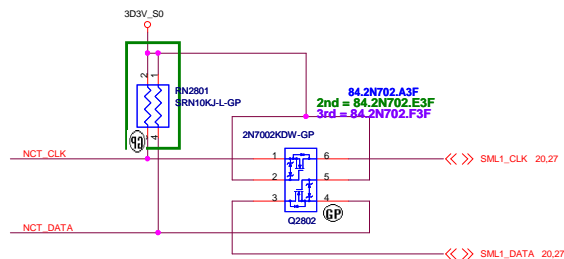
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Title <div>Clock(colay)</div>		
Size <div>A4</div>	Document Number <div>Angel-CY</div>	Rev <div>1</div>
Date <div>Monday, April 22, 2013</div>		Sheet <div>26</div> of <div>102</div>

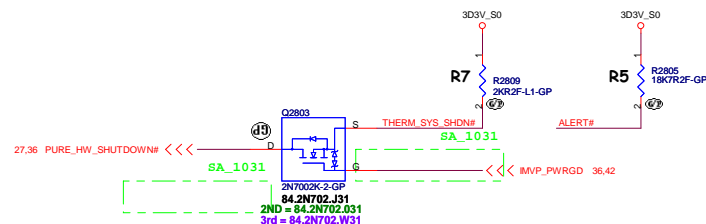


2. System Sensor, Put on palm test



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	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C
T CRIT temperature strapping point					



Title			
Thermal Sensor NCT7718W			
Size	Document Number	Rev	
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Title			
Audio Codec ALC3225			
Size	Document Number	Rev	
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AUDIO OP AMPLIFIER

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Title <div>Audio AMP</div>		
Size <div>A4</div>	Document Number <div>Angel-CY</div>	Rev <div>1</div>
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Title		
AR8158		
Size	Document Number	Rev
A4	Angel-CY	1
Date:	Monday, April 22, 2013	Sheet 31 of 102

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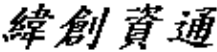
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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Angel-CY</div>	Rev <div>1</div>
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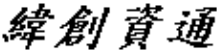
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Reserved			
Size A4	Document Number Angel-CY		Rev 1
Date: Monday, April 22, 2013		Sheet 34 of	102

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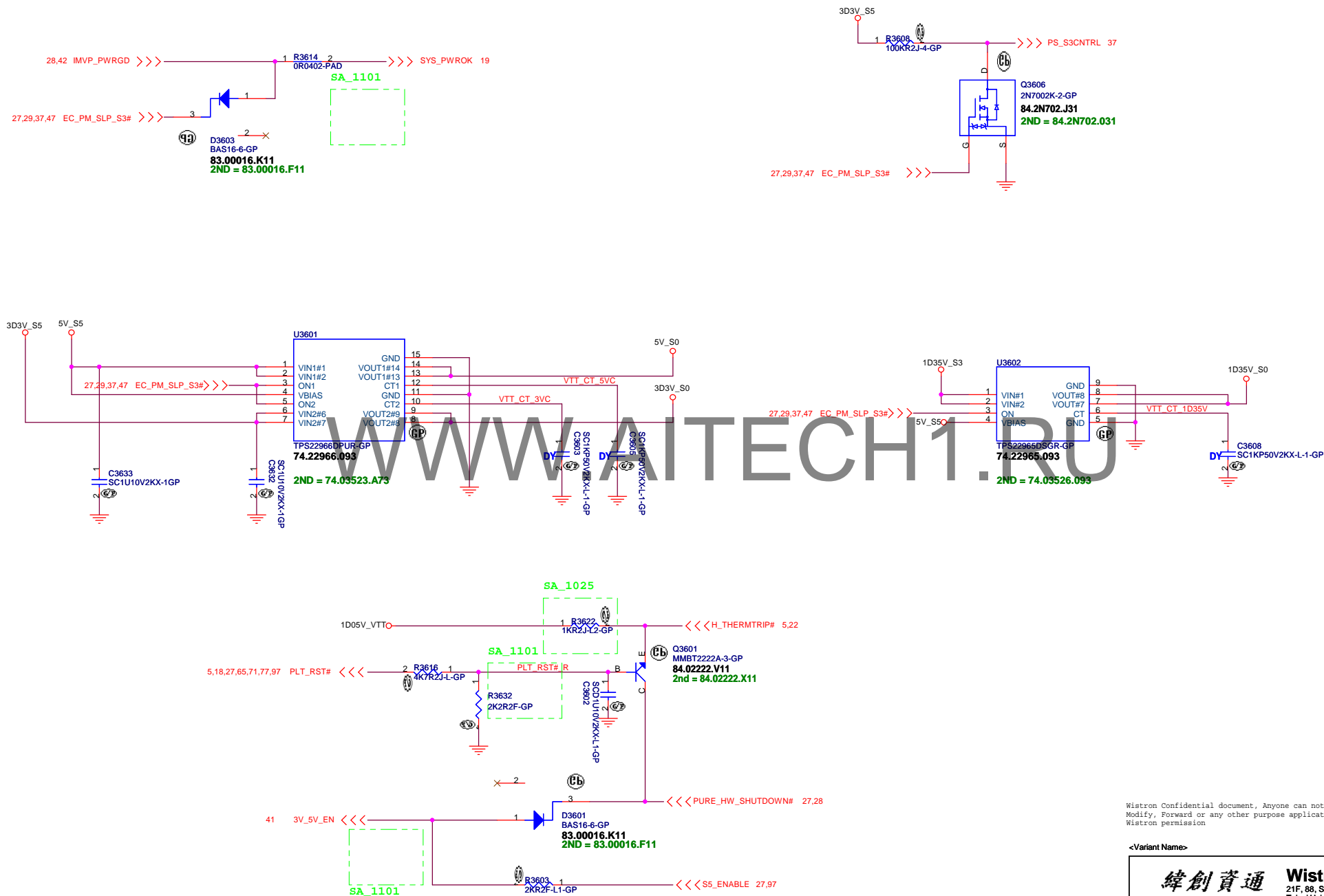
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USB 3.0 Controller			
Size A4	Document Number Angel-CY		Rev 1
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Power Sequence



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SA_1101

Q3708
AO3418L-GP

10k

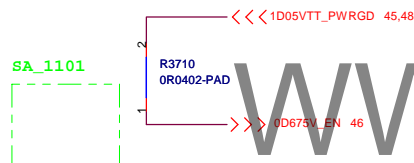
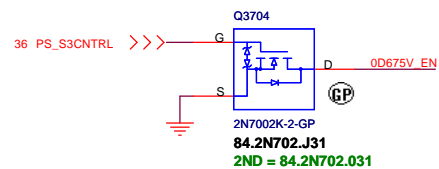
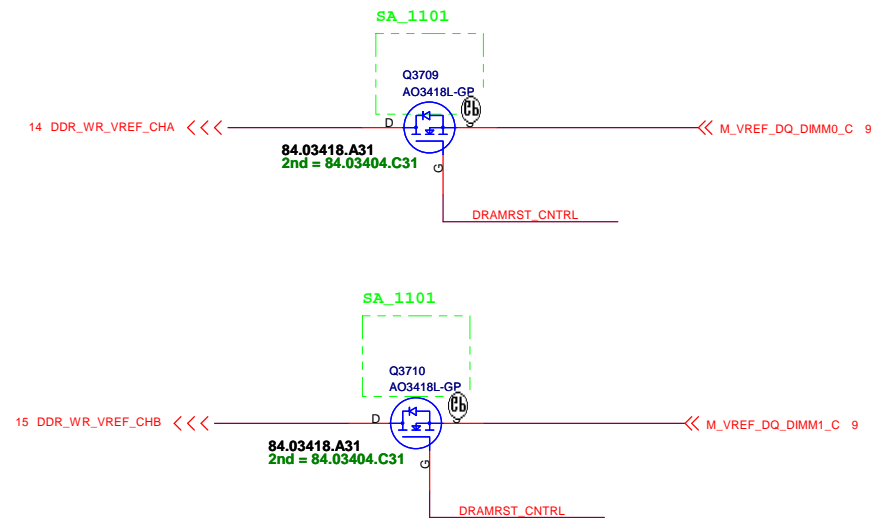
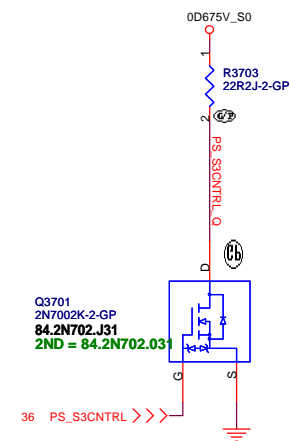
R3705
100KR2J-4-GP

DDR_VREF_S3

84.03418.A31
2nd = 84.03404.C31

>>> +V_SM_VREF_CNT 9

EC_PM_SLP_S3# 27,29,36,47

[illegible][illegible]

<Variant Name>

Title			
ADAPTER			
Size A3	Document Number		Rev
	Angel-CY		1
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remember to check pin define

The schematic diagram illustrates a complex power management circuit. Key components and sections include:

- DCIN1 Section:** Features an ACES-CONS-27-GP component, a DC input (AD_JK_IN), and a network of capacitors (PC3812, PC3813) and diodes (PD3801, PD3802).
- 2/26 wayler Section:** Includes a SC1U25V3KX-1-GP component and a network of resistors (PR3801, PR3802, PR3803, PR3804, PR3805) and capacitors (PC3801, PC3802).
- 27 AD_OFF Section:** Features an LTC024EUB-1-GP component and a network of resistors (R1, R2) and capacitors (PC3801, PC3802).
- 27 AD_2ND_BATT Section:** Includes a TPC8131-GP component and a network of resistors (PR3818, PR3816, PR3817) and capacitors (PC3818, PC3819).
- Other Components:** Various transistors (PQ3801, PQ3802, PQ3803, PQ3804, PQ3805), diodes (PD3801, PD3802, PD3803, PD3804), and capacitors (PC3801, PC3802, PC3803, PC3804, PC3805) are distributed throughout the circuit.

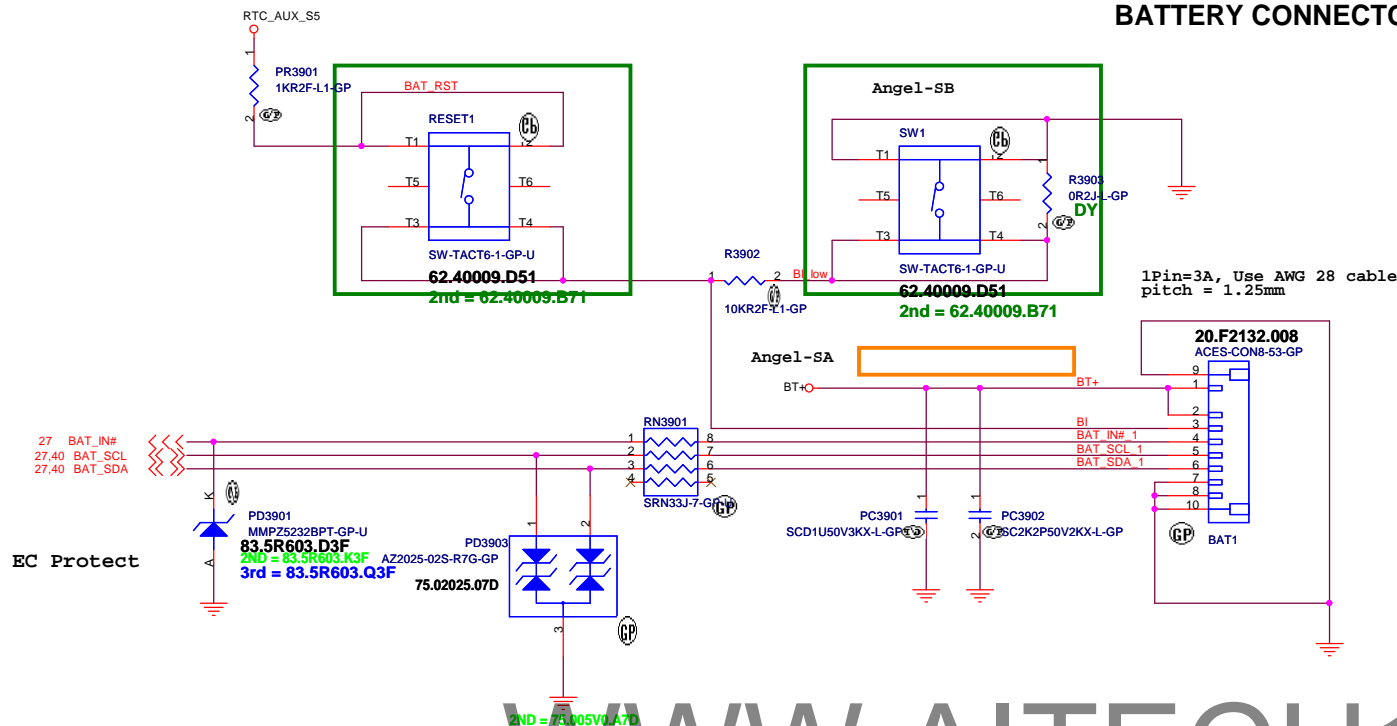
A large watermark "WWW.AITECH1.RU" is overlaid across the center of the diagram.

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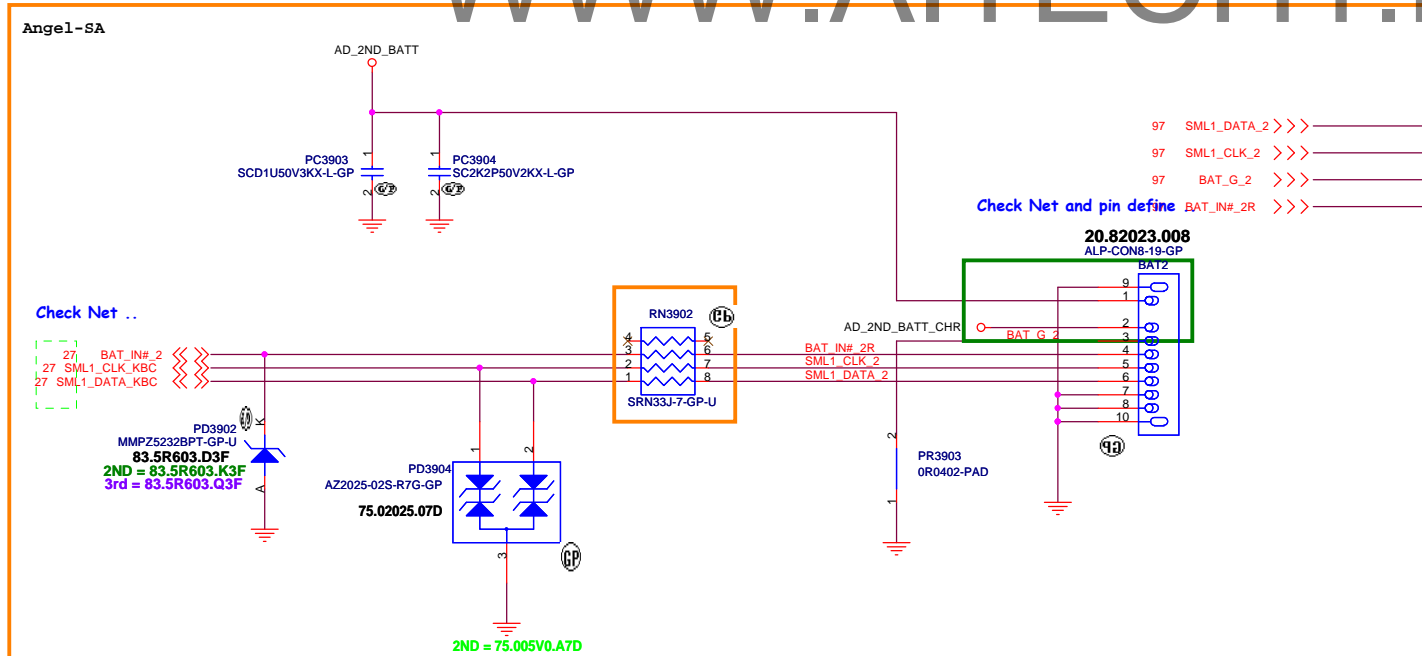
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Title			
DCIN JACK			
Size A3	Document Number		Rev 1
Angel-CY			
Date:	Monday, April 22, 2013	Sheet 38 of	102

BATTERY CONNECTOR



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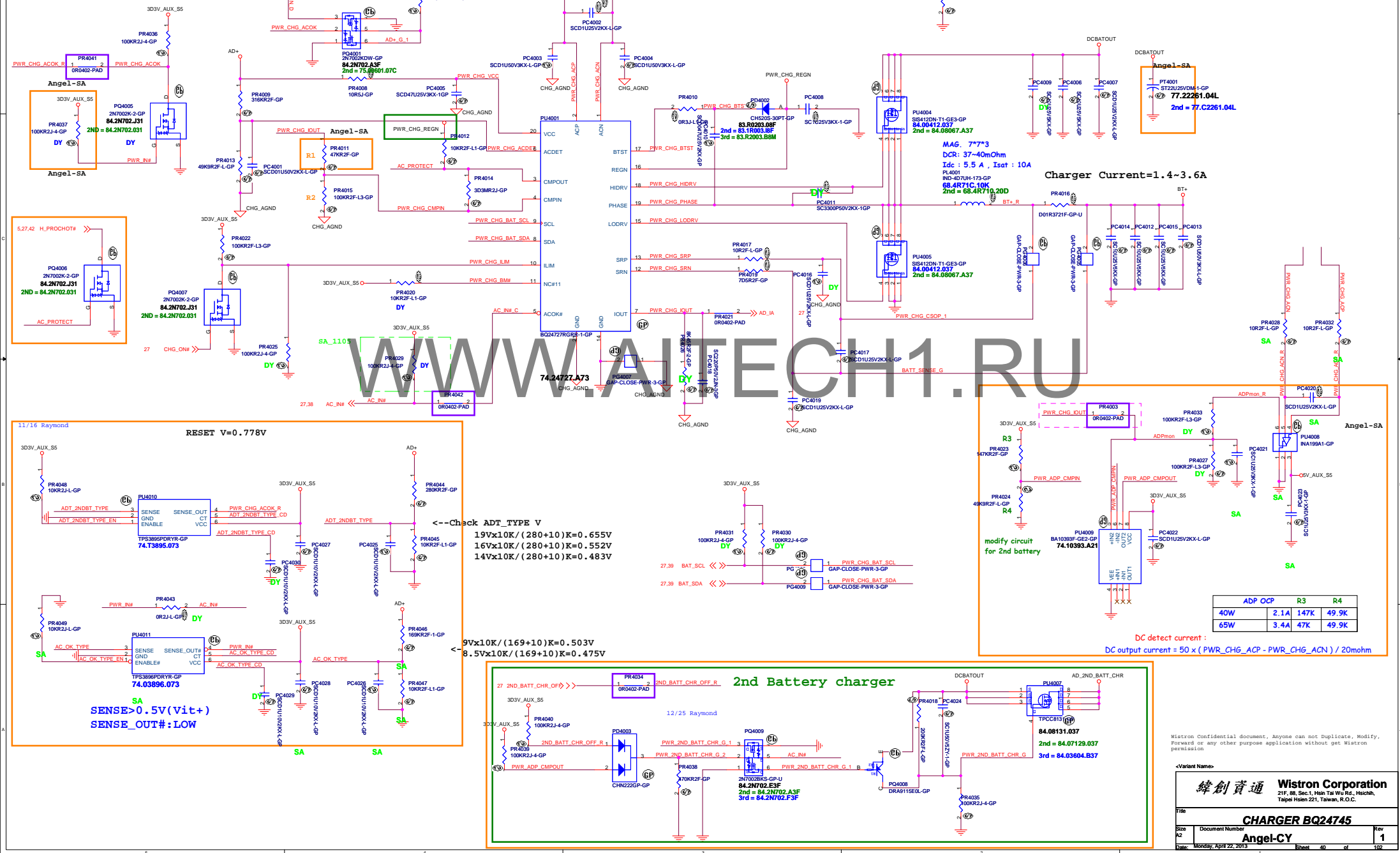
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Title	BATT CONN
Size A3	Document Number Angel-CY
Date: Monday, April 22, 2013	Rev 1
Sheet 39	of 102

SSID = Charger

AD+ total power	R1	R2
40w	47K	100K
65w	137K	100K



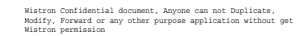
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Title			
CHARGER BQ24745			
Size A2	Document Number		Rev
	Angel-CY		1
Date:	Monday, April 22, 2013		Sheet 40 of 102

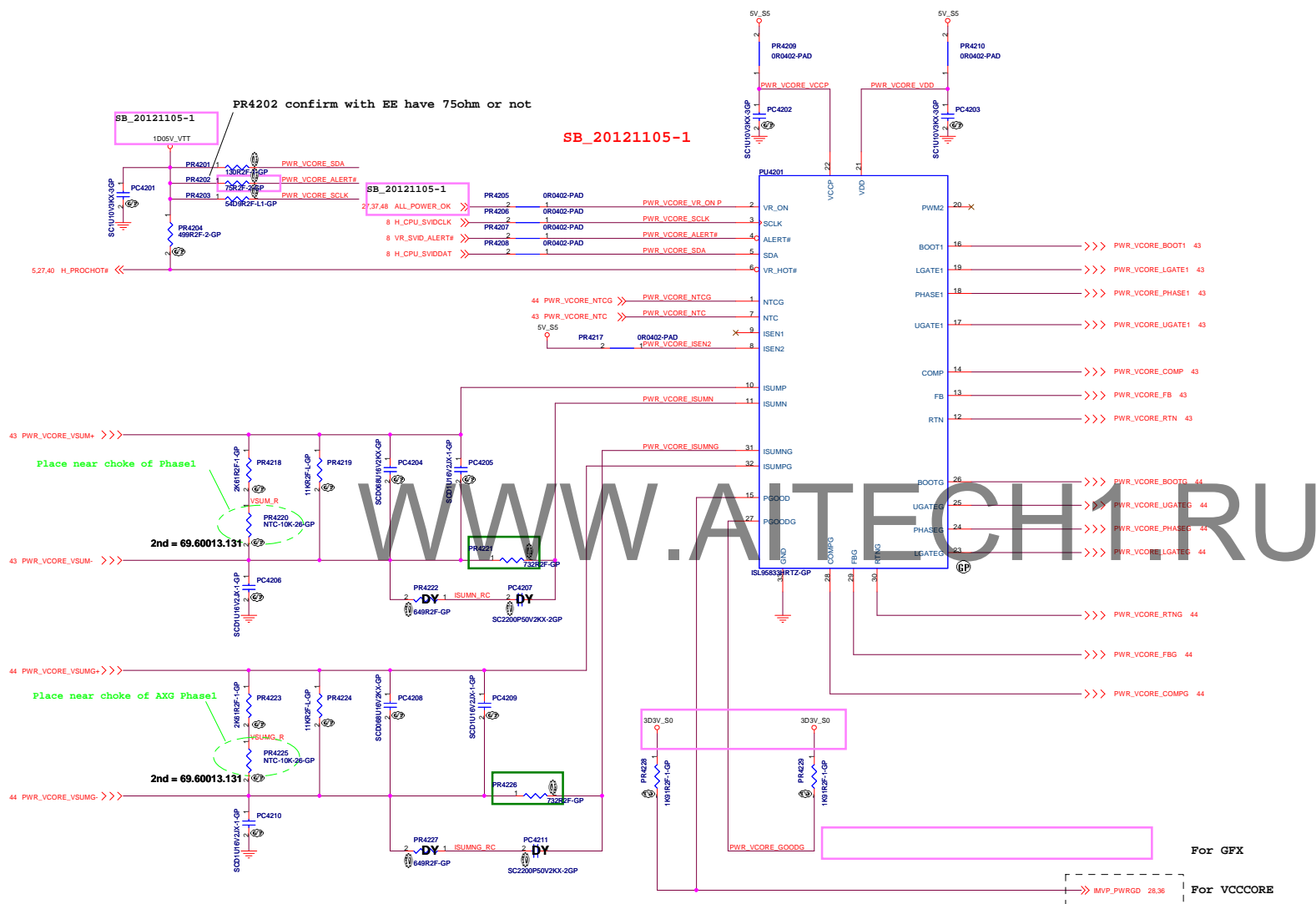
check (UVP)



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Title			
TPS51125A 5V/3D3V			
Size	Document Number		Rev
Custom	Angel-CY		1
Date:	Monday, April 22, 2013	Sheet 41 of	102

SSID = CPU.Regulator

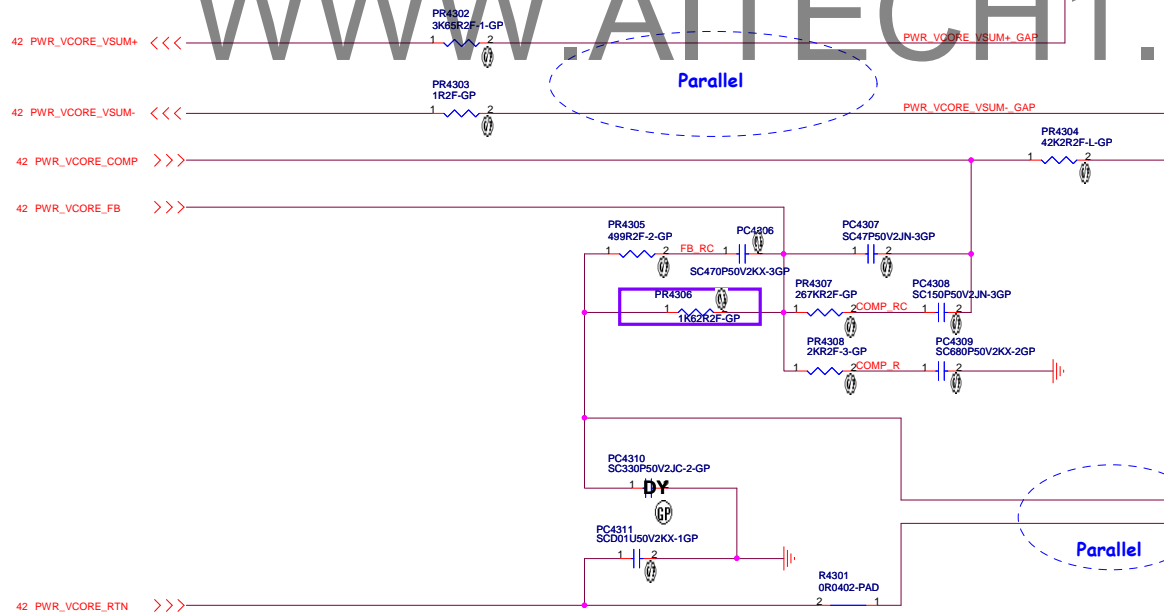
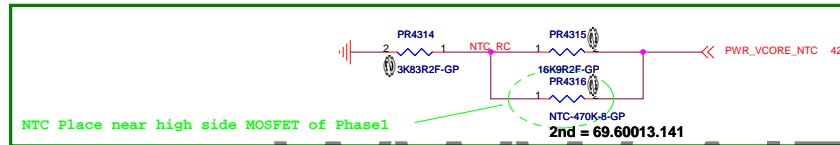
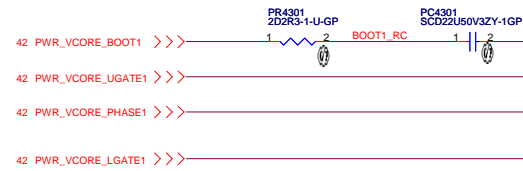
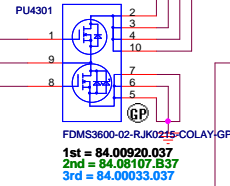


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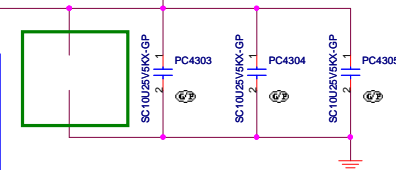
BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDM33664S)	Mount
PU4302	84.03664.037 (FDM33664S)	DY

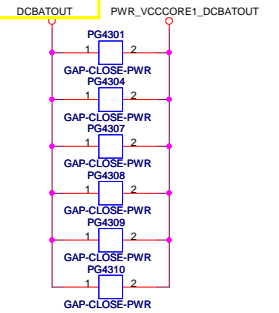
BOM control



PWR_VCCCORE1_DCBATOUT

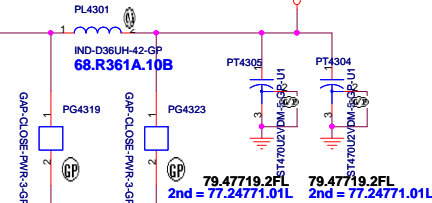


SA_20121019

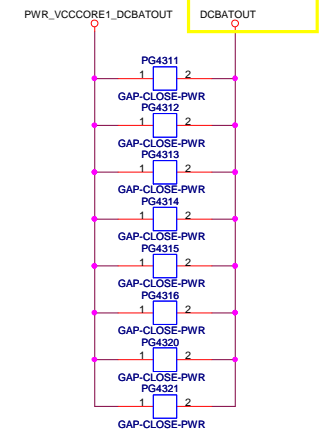


Pana . 7 x 7 x 4
DCR 1.8~2.3 mOhm
Isat : 32 A

VCC_CORE



SA_20121019



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UMA C

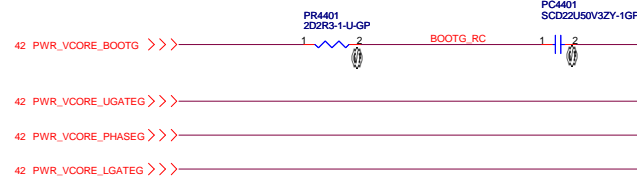
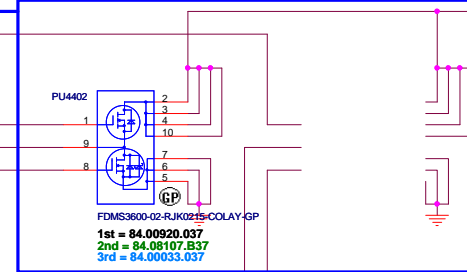
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Size	Document Number
Custom	Angel-CY
Date	Monday, April 22, 2013
Sheet	43 of 103
Rev	1

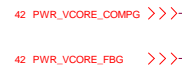
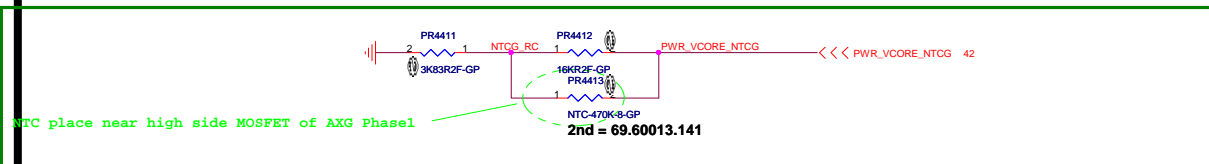
BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S)	Mount
PU4402	84.03664.037 (FDMS3664S)	DY

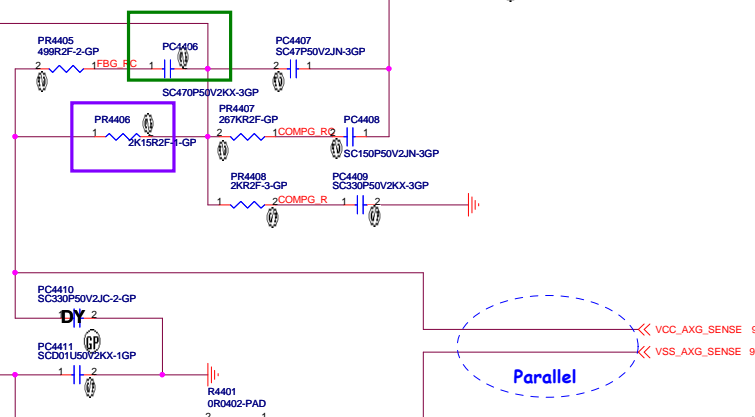
BOM control



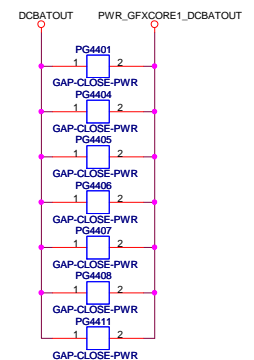
Pana . 7 x 7 x 4
DCR 1.8~2.3 mOhm
Isat : 32A



AXG	Loadline	PR4064
GT1	4.6mohm	237ohm
GT2	3.9mohm	432ohm

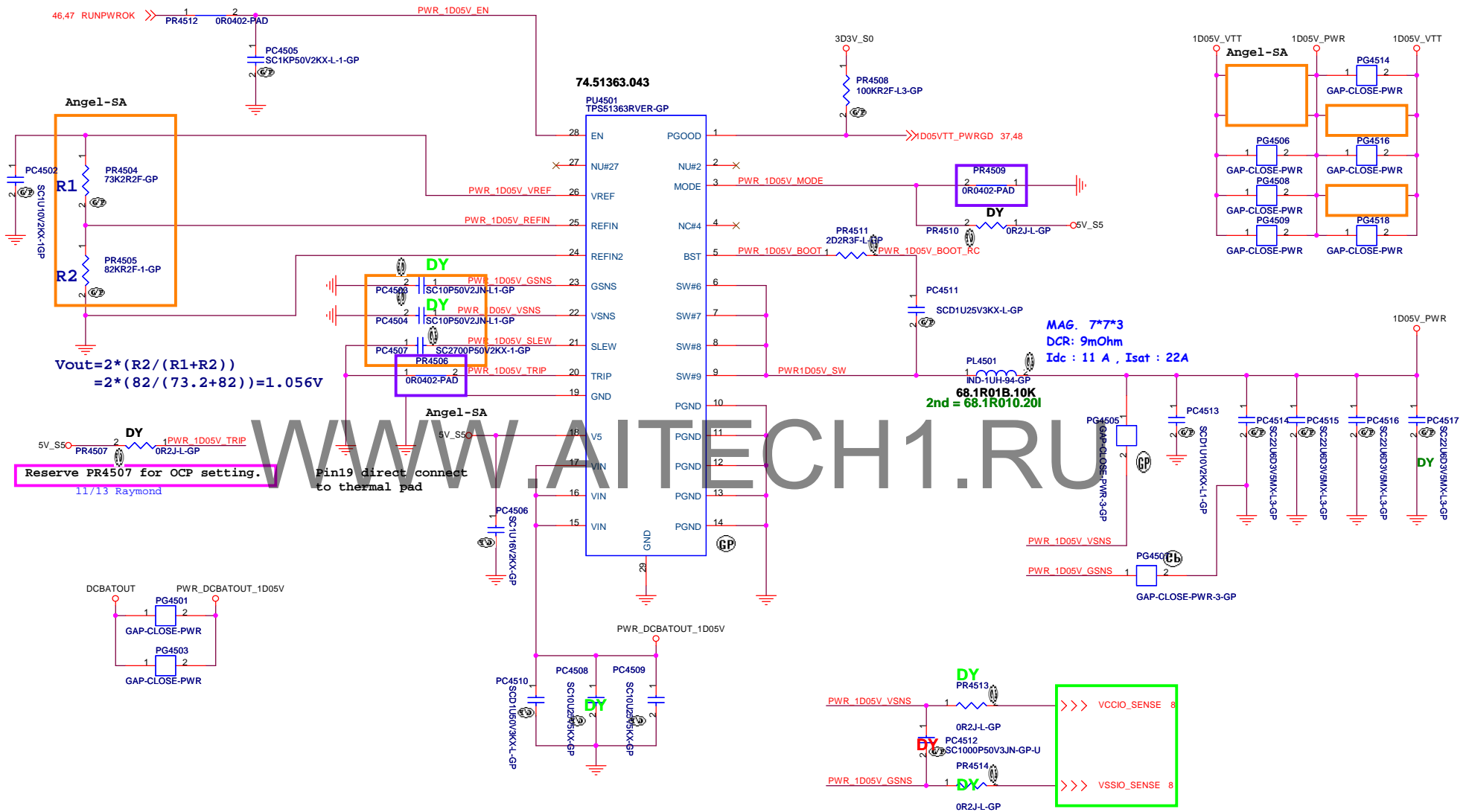


79.33719.2EL 79.33719.2EL



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TPS51363 for 1D05V



HR PX

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Title

DC to DC 1D05V(TPS51218D)

Size
A3

Size	Document Number
A3	A

Date: Monday, April 22, 2013

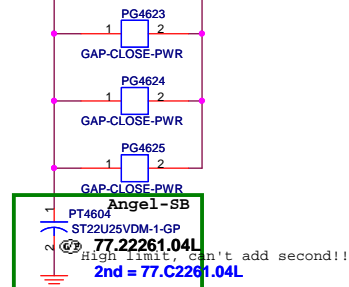
Angel-CY

Rev
1

SSID = PWR.Plane.Regulator_lp35v0p675v

RT8207L for VDDQ

DCBATOUT PWR_ID35V_DCBATOUT



Angel-SA

PU4605
SIS412DN-T1-GE3-GP
84.00412.037
2ND = 84.08067.A37

PWR_VDDQ_UGATE

PWR_VDDQ_PHASE

PWR_VDDQ_LGATE

PU4603
SIS780DN-T1-GE3-GP
84.00780.037
2ND = 84.08065.B37

PU4601
RT8207MZQW-GP-U
74.08207.C73
2nd = 74.01566.073

CYNTEC. 0.68uH 7*7*3
DCR= 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A

Icc_Max:11A
TDC: 8.8A
OCP:14.3A

PL4601
IND-D68UH-36-GP
68.R681A.10A
2nd = 68.R6810.20J

PT4601
SE330U2D5VM-8-GP
77.53371.18L

+0.675VS
Iomax: 1.2A

Iomax=1A
OCP>1.5A

Close to output cap pin1, not
inside of the output cap
 $V_{out} = 0.75 \times (1 + R1/R2)$
 $= 0.75 \times (1 + 40/49.9)$
 $= 1.35$

Close to PIN9

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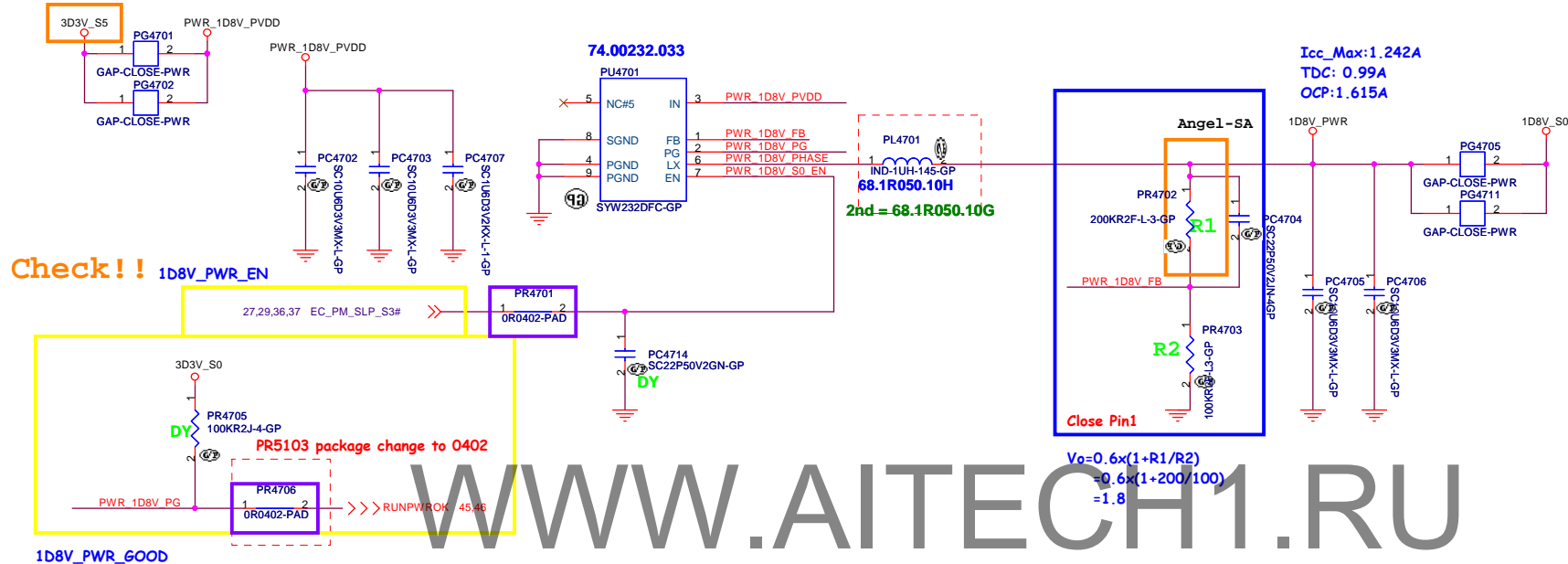
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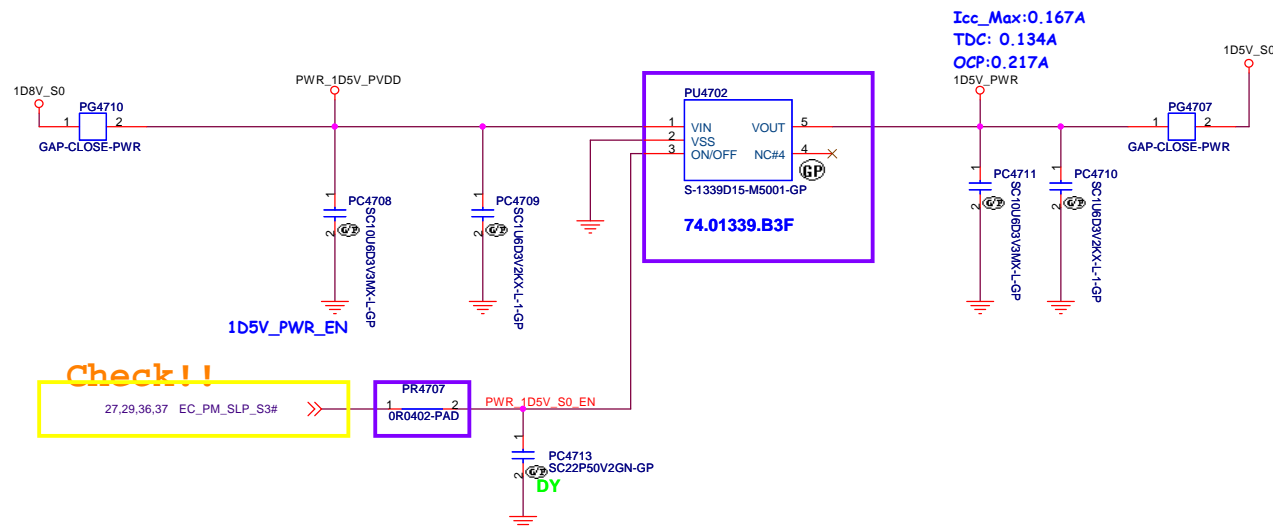
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Size			Document Number	Rev
A3			Angel-CY	1
Date:			Monday, April 22, 2013	Sheet 46 of 102

SSID = PWR.Plane.Regulator_1p8v

Check!!



S-1339D15 for +1.5V



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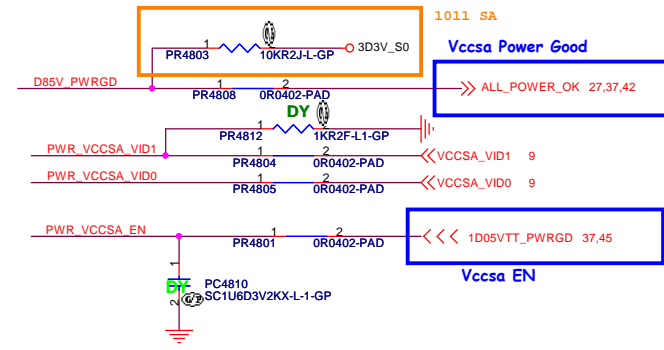
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Title DC CONVERTER_1D8V&1D5V

Size A3 Document Number Angel-CY Rev 1

Date: Monday, April 22, 2013 Sheet 47 of 102

LDO G978 for VCCSA



D0, D1 V_O Selection Table

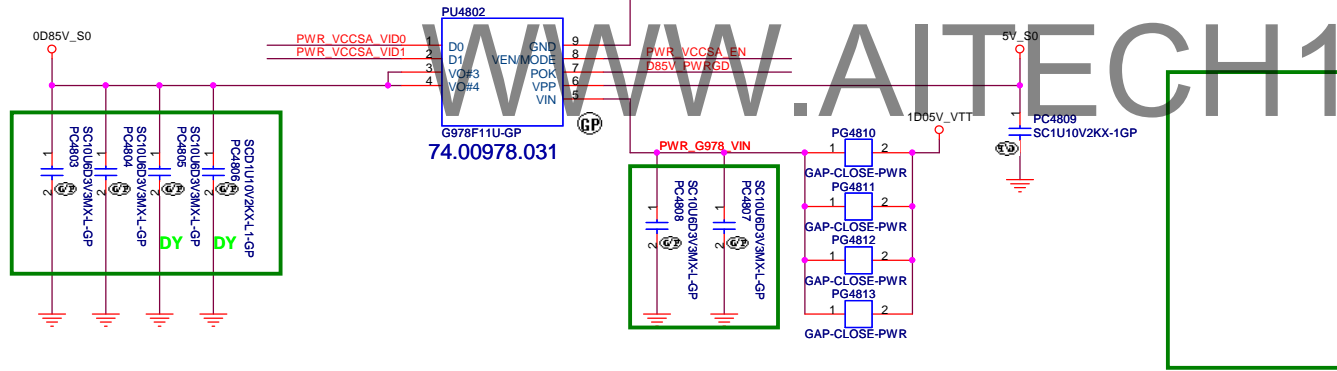
D0	D1	V _O MODE=0	V _O MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

"X" means "don't care".

VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic	VEN/MODE (VPP=5V)	MODE logic
<0.6V	0	<2.0V	0
>1.0V	1	>2.6V	1

Design Current =4 A



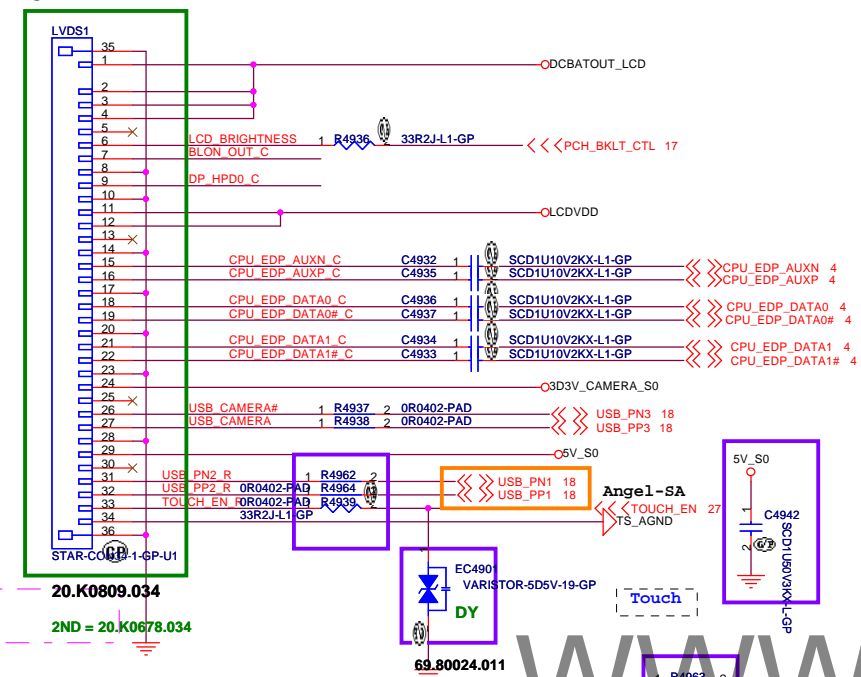
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UMA C

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Title VCCSA LDO G978	
Size A3	Document Number Angel-CY
Date: Monday, April 22, 2013	Sheet 48 of 103

SSID = VIDEO

Angel-SA



J1 Pin Assignment	
1	USB5V
2	D-
3	D+
4	GND
5	GND
6	INT

```

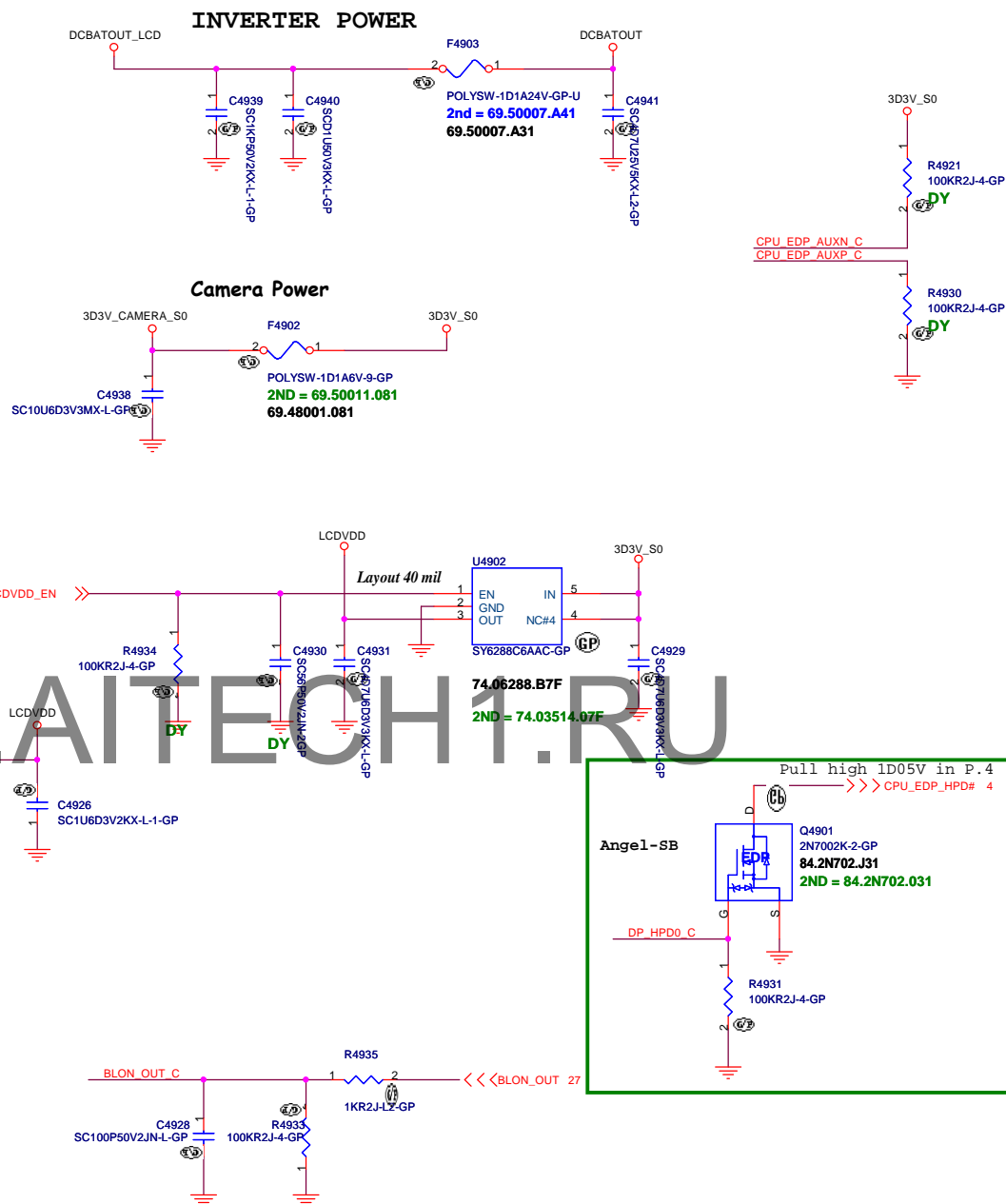
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97 BLON_OUT_C >>>_____

97 LCD_BRIGHTNESS >>>_____
97 CPU_EDP_DATA1_C >>>_____
97 CPU_EDP_DATA1#_C >>>_____
97 CPU_EDP_DATA0_C >>>_____
97 CPU_EDP_DATA0#_C >>>_____

97 CPU_EDP_AUXP_C >>>_____
97 CPU_EDP_AUXN_C >>>_____

```

For AFTE



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Title

LCD Connector

Size
A3

Document Number

Angel-CY

Date: Monday, April 22, 2013

Sheet 49

Rev	1
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Title <div>CRT Connector</div>		
Size <div>A4</div>	Document Number <div>Angel-CY</div>	Rev <div>1</div>
Date <div>Monday, April 22, 2013</div>		Sheet <div>50</div> of <div>102</div>

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Title			
HDMI Level Shifter/Connector			
Size	Document Number		Rev
A3	Angel-CY		1
Date:	Monday, April 22, 2013	Sheet	51 of 102

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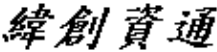
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
S-VIDEO		
Size	Document Number	Rev
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Title			
Reserved			
Size A4	Document Number Angel-CY		Rev 1
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SSID = User.Interface

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Title

ITP

Size
A4

Document Number

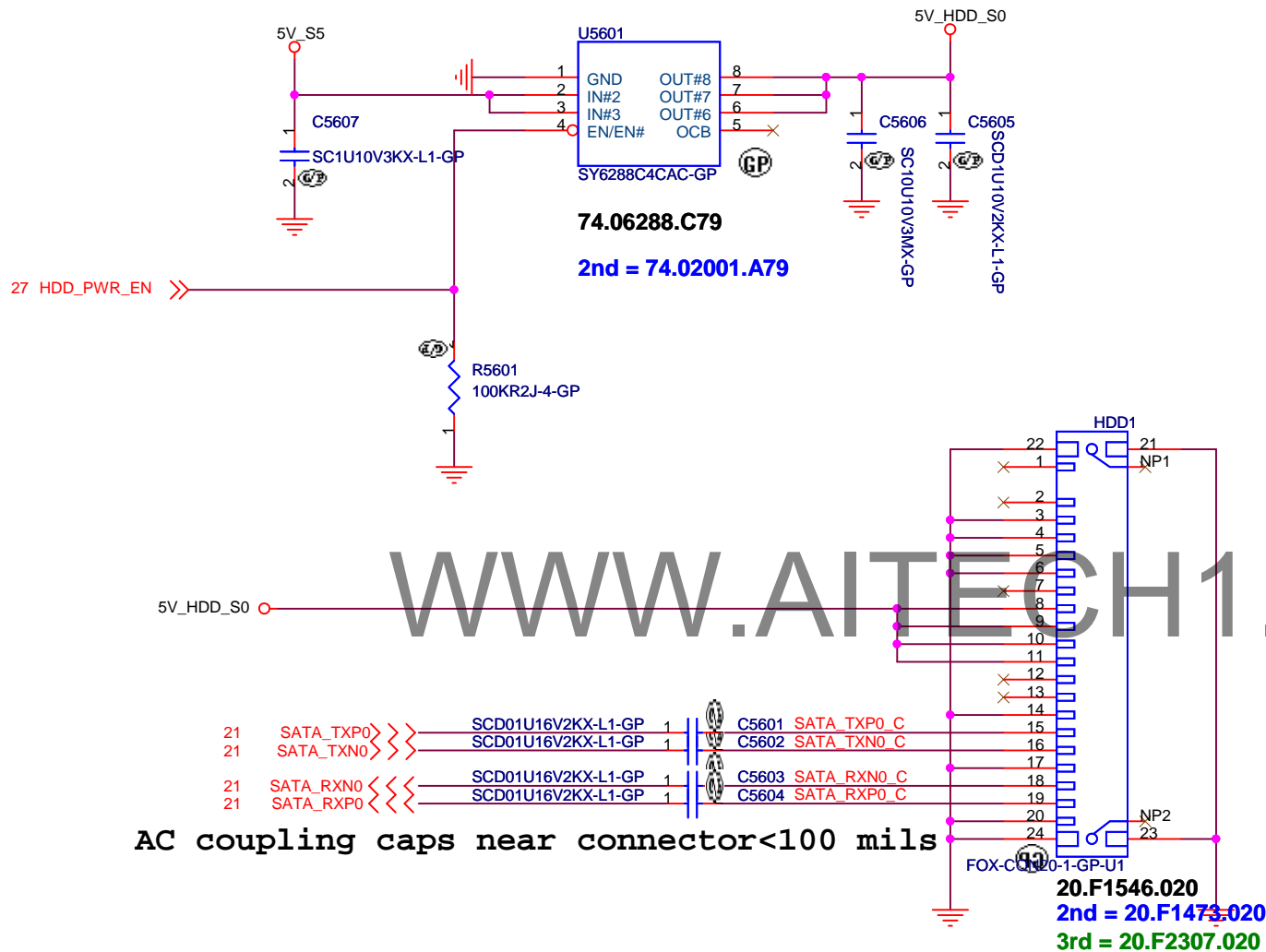
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1

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SATA HDD Connector



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Title			
HDD			
Size A4	Document Number Angel-CY		Rev 1
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Title		
E-SATA/USB CHARGER		
Size	Document Number	Rev
A4	Angel-CY	1
Date:	Monday, April 22, 2013	Sheet 57 of 102

SSID = AUDIO

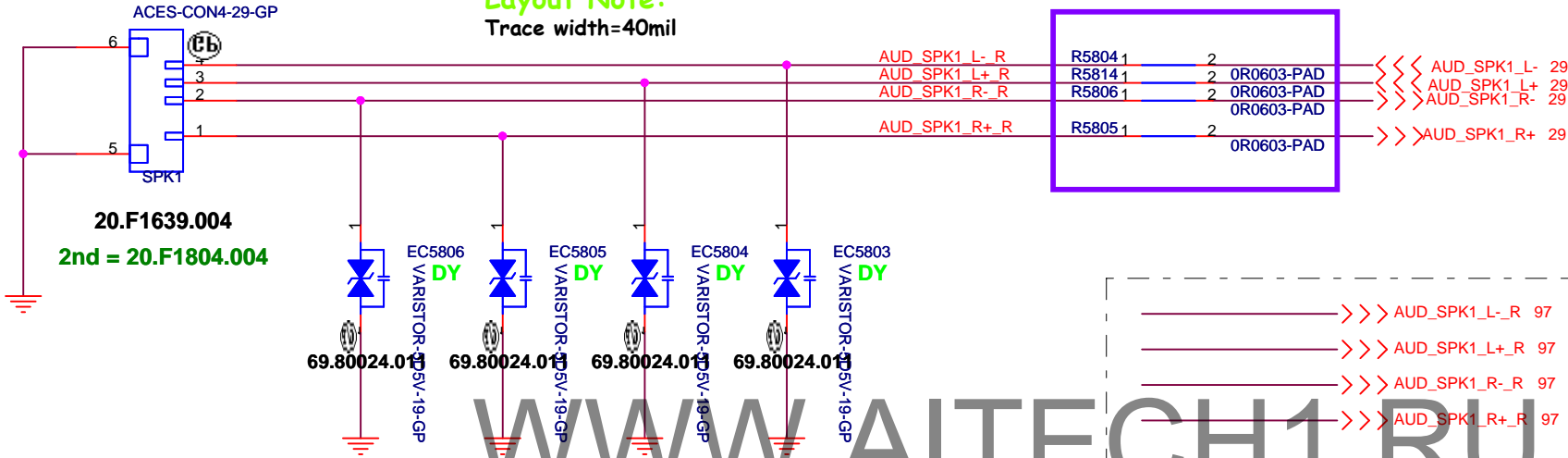
SSID = AUDIO

Speaker

SA
10/22 change by Edwin
Pin Define SWAP

Layout Note:

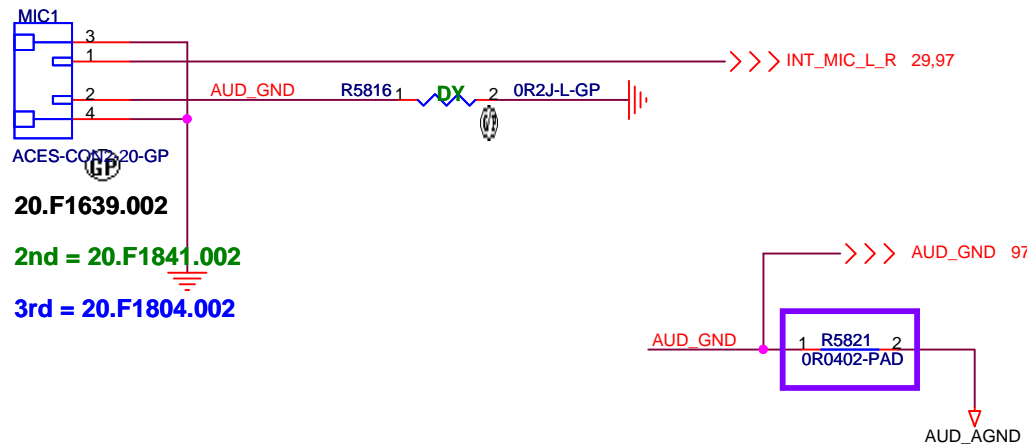
Trace width=40mil



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Combo Jack on Small Board

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Title

MIC/SPEAKER/JACK

Size
A4

Document Number

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1

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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

Blanking

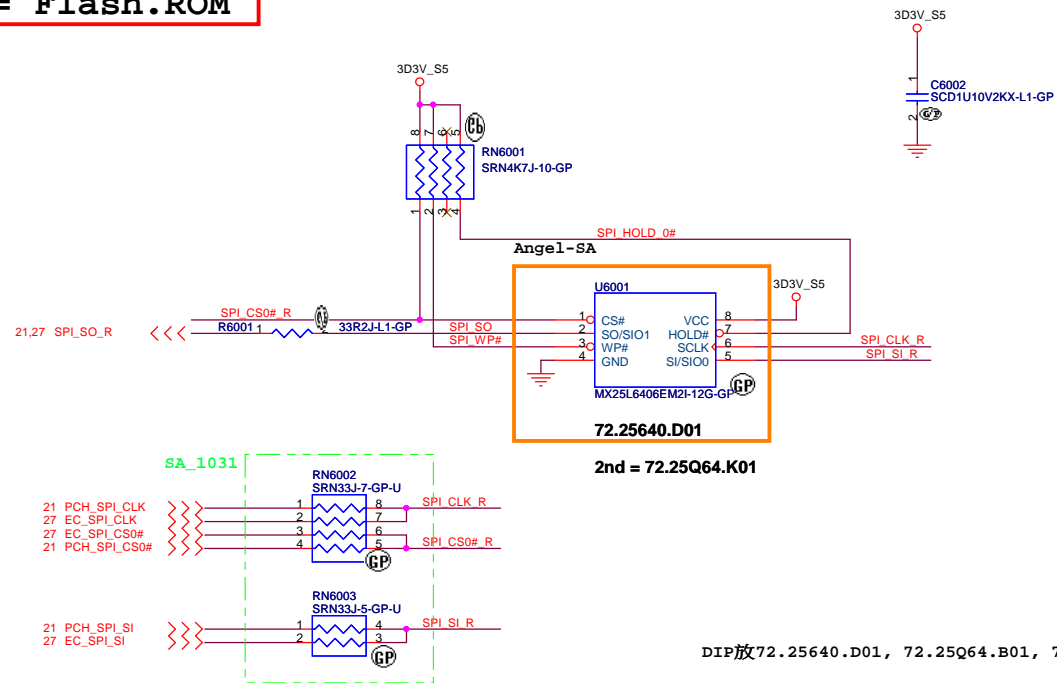
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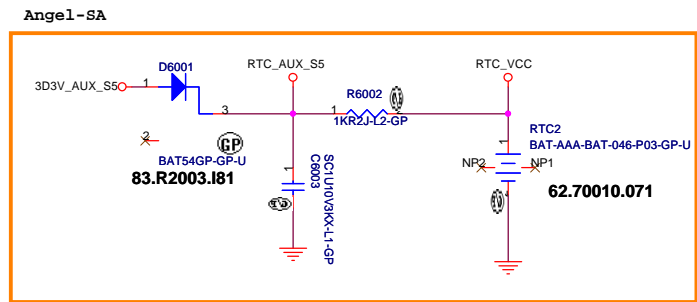
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		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>LAN CONNECTOR</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A4</div>	<div>Angel-CY</div>		<div>1</div>
<div>Date</div>		<div>Monday, April 22, 2013</div>	<div>Sheet 59 of 102</div>

SSID = Flash.ROM



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SSID = RBATT



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Title Flash/RTC		
Size Custom	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 60 of 102	

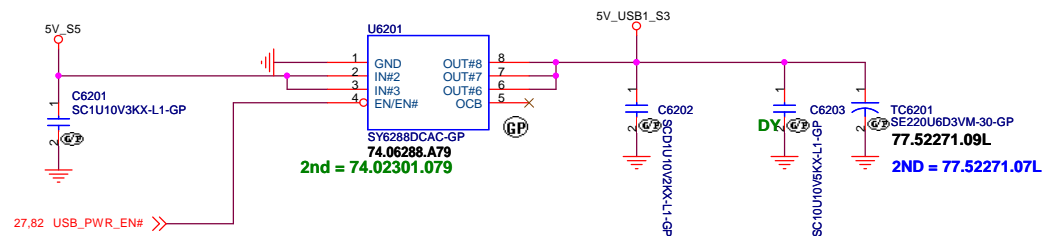
SSID = USB

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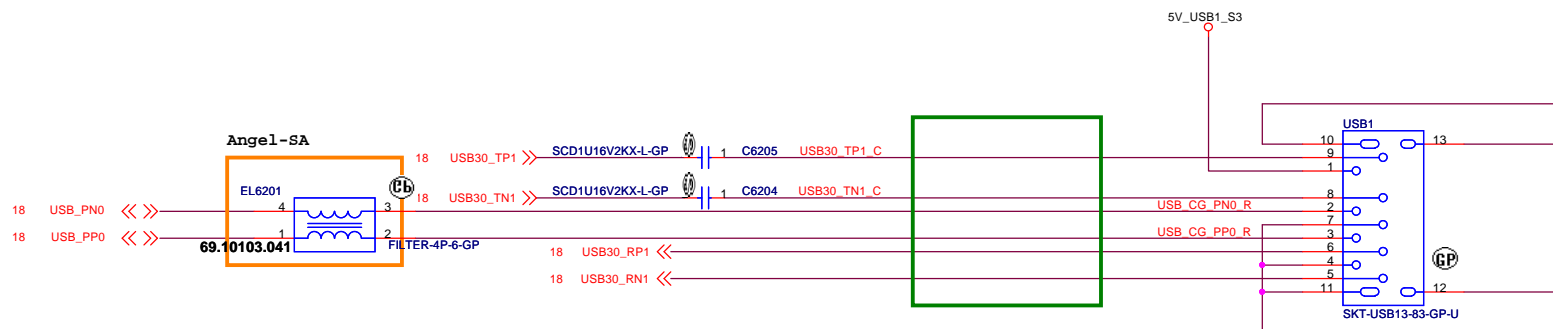
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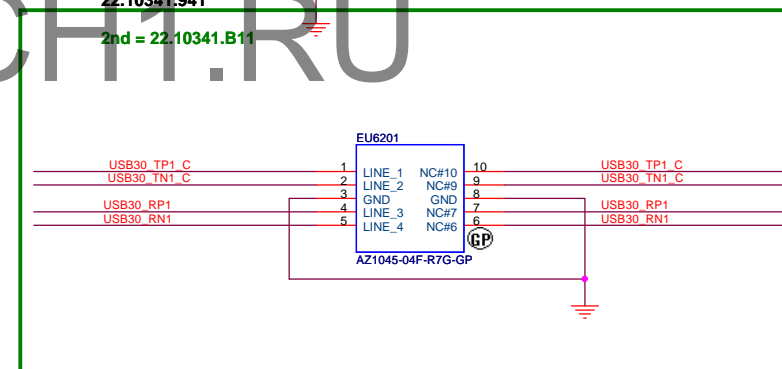
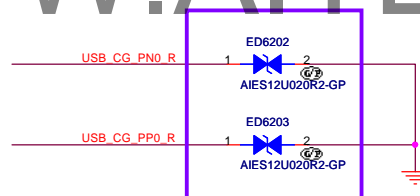
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>USB Power SW</div>		
Size <div>A4</div>	Document Number <div>Angel-CY</div>	Rev <div>1</div>
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USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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USB 3.0 Port	
Title Size A3 Date: Monday, April 22, 2013	Document Number Angel-CY Sheet 62 of 102
Rev 1	

SSID = User.Interface
Bluetooth Module conn.

Without BT

Blanking

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Title

Bluetooth

Size
A4

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1

Date: Monday, April 22, 2013

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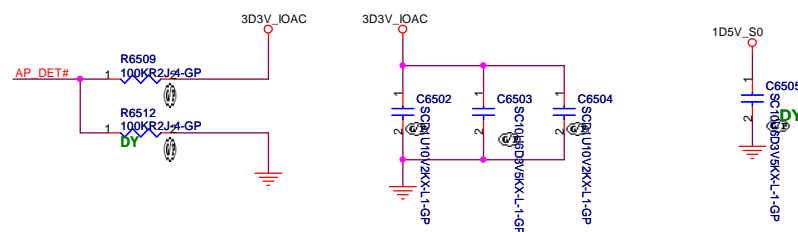
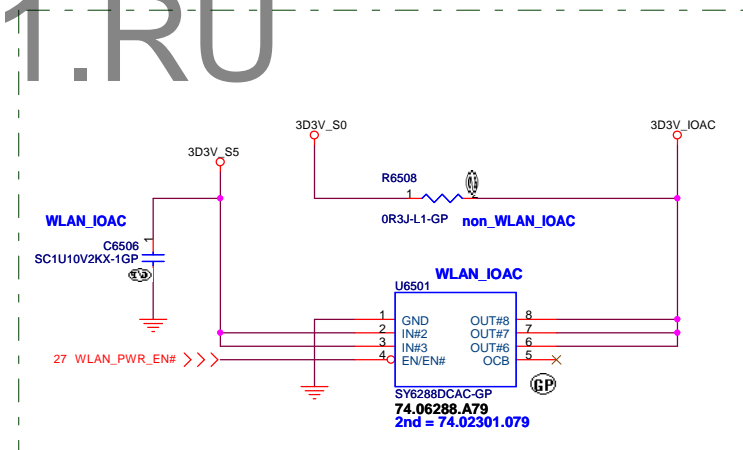
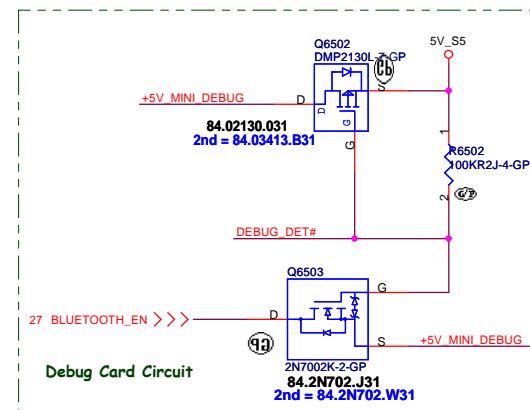
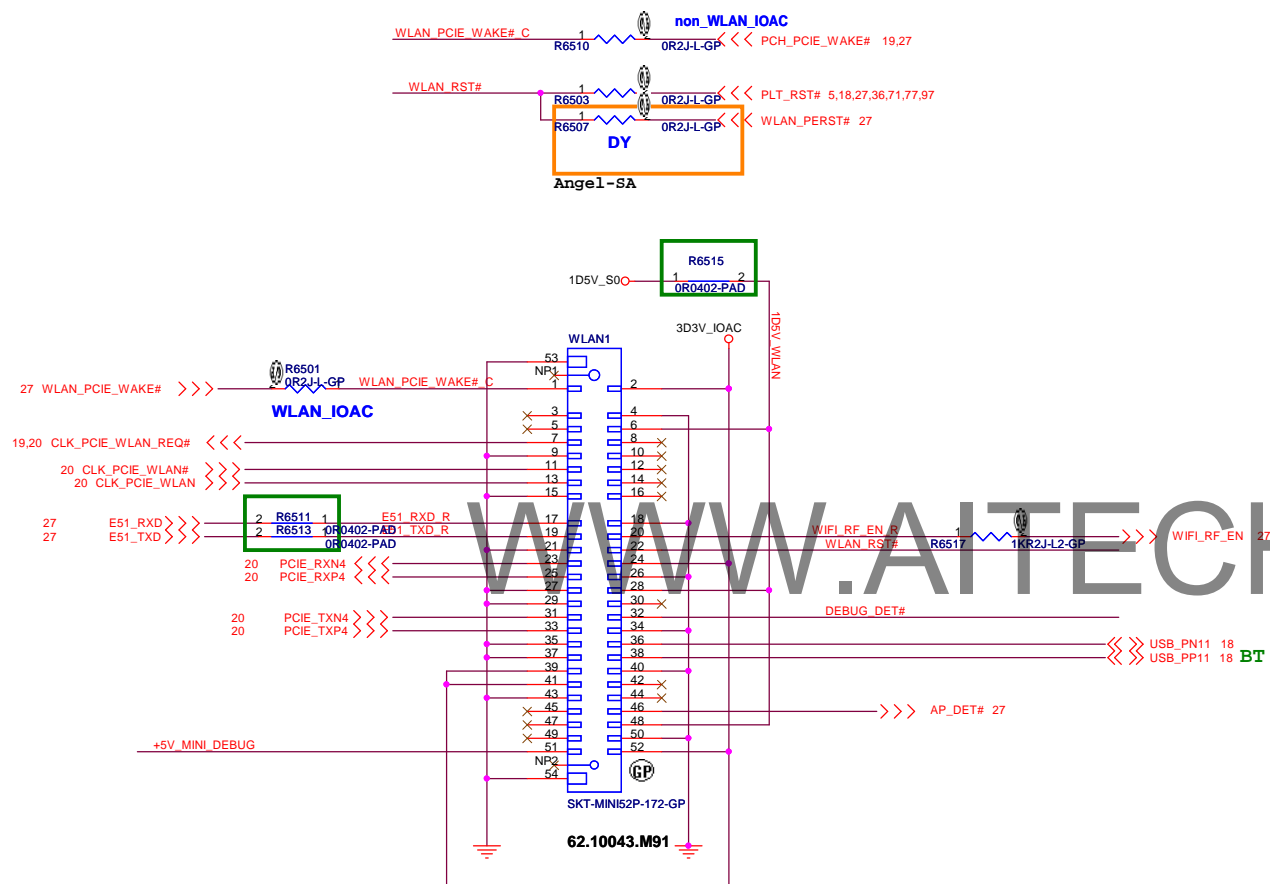
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Title <div>RESERVED</div>		
Size <div>A4</div>	Document Number <div>Angel-CY</div>	Rev <div>1</div>
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SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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Title	MINICARD(WLAN)	
Size A3	Document Number	Rev 1
Date: Monday, April 22, 2013	Sheet 65 of 102	

SSID = Wireless

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Title			
WWAN Connector			
Size	Document Number		Rev
A4	Angel-CY		1
Date: Monday, April 22, 2013		Sheet 66 of	102

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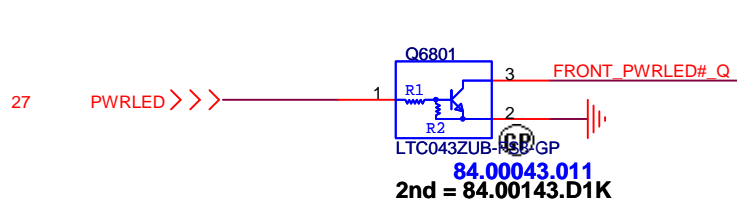
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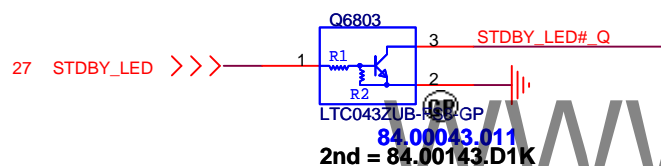
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
M-SATA		
Size	Document Number	Rev
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SSID = User.Interface

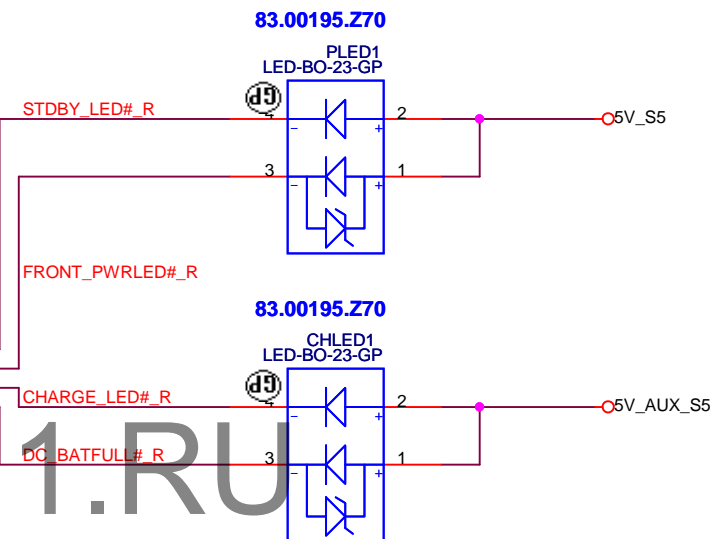
Power button LED



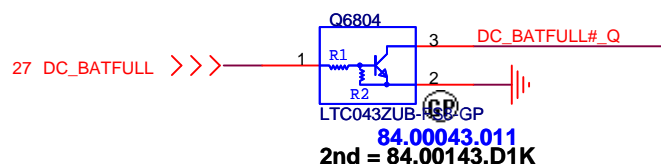
Power STDBY_LED



STDBY_LED#_Q	1	R6801	560R2F-GP
FRONT_PWRLED#_Q	1	R6802	300R2F-GP
CHARGE_LED#_Q	1	R6803	560R2F-GP
DC_BATFULL#_Q	1	R6804	300R2F-GP



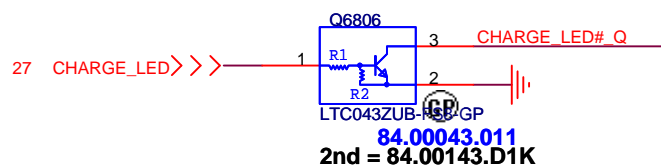
Battery LED2 (DC_BATFULL)



Devices

Part No.	Lens	Source Color	Pin Assignment
LTST-C195ZBKFKT	Water Clear	InGaP Blue	1,3
		AlInGaP Orange	2,4

Battery LED1 (CHARGE)



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<Variant Name>

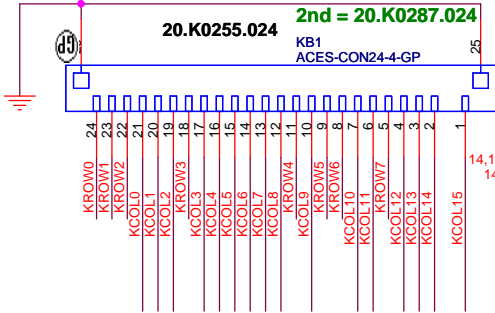
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
LED Bard/Power Button			
Size	Document Number		Rev
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TOUCH PAD

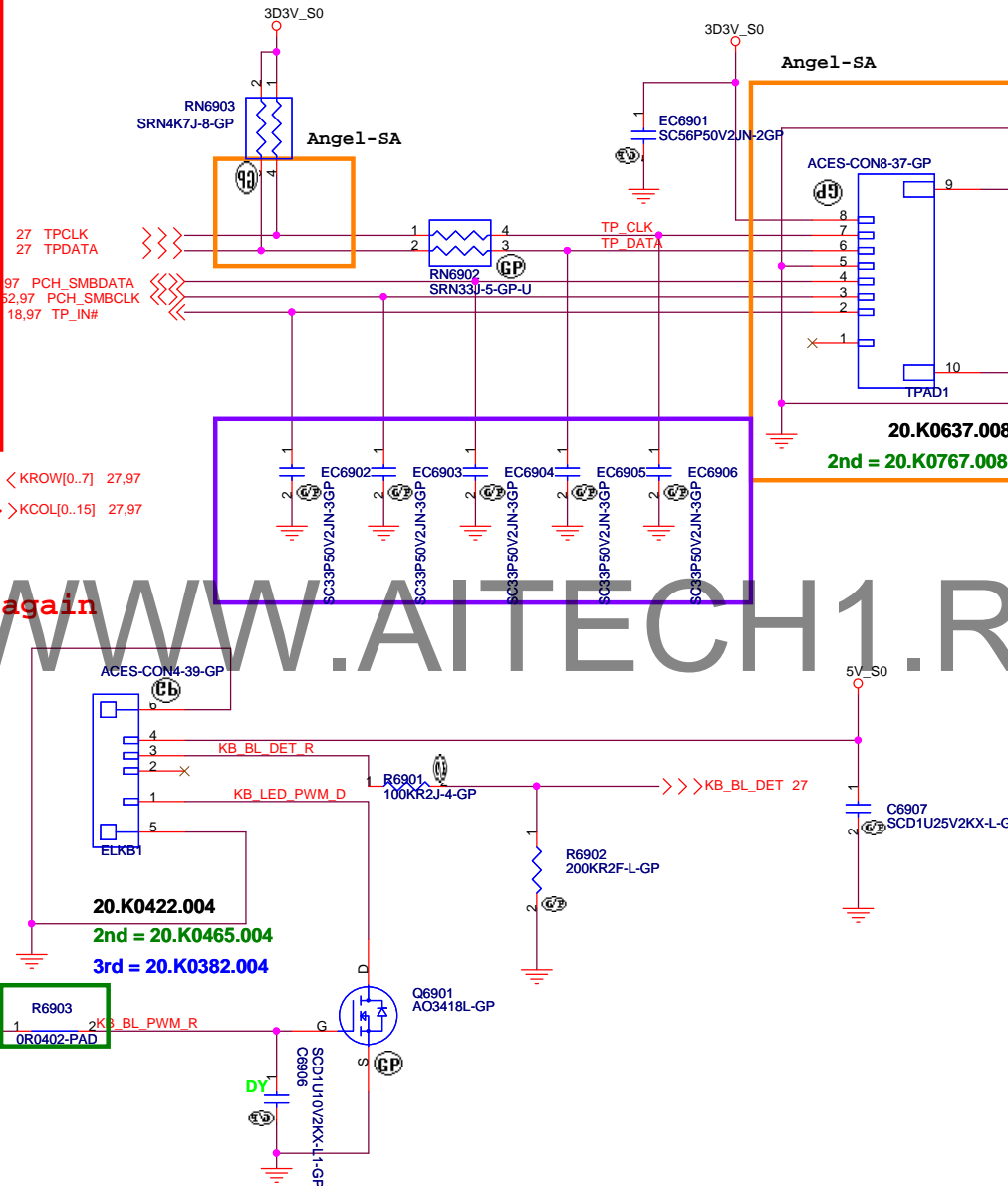
D = KBC

Internal KeyBoard Connector

上接觸



KB Pin define need to check again



27,97	KCOL0	>>>
27,97	KCOL1	>>>
27,97	KCOL2	>>>
27,97	KCOL3	>>>
27,97	KCOL4	>>>
27,97	KCOL5	>>>
27,97	KCOL6	>>>
27,97	KCOL7	>>>
27,97	KCOL8	>>>
27,97	KCOL9	>>>
27,97	KCOL10	>>>
27,97	KCOL11	>>>
27,97	KCOL12	>>>
27,97	KCOL13	>>>
27,97	KCOL14	>>>
27,97	KCOL15	>>>

27,97	KROW0	>>>
27,97	KROW1	>>>
27,97	KROW2	>>>
27,97	KROW3	>>>
27,97	KROW4	>>>
27,97	KROW5	>>>
27,97	KROW6	>>>
27,97	KROW7	>>>
97	TP_DATA	>>>
97	TP_CLK	>>>

For AFTE

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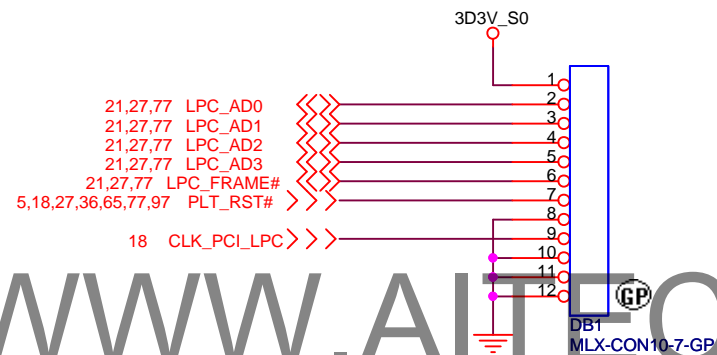
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Title Key Board/Touch Pad		
Size Custom	Document Number Angel-CY	Rev 1
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<Variant Name>

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DB

1st = 20.F0714.010

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Title					
Dubug connector					
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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Angel-CY</div>	Rev <div>1</div>
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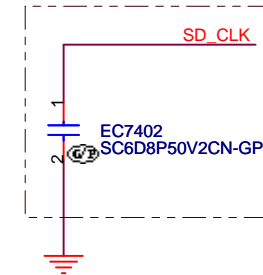
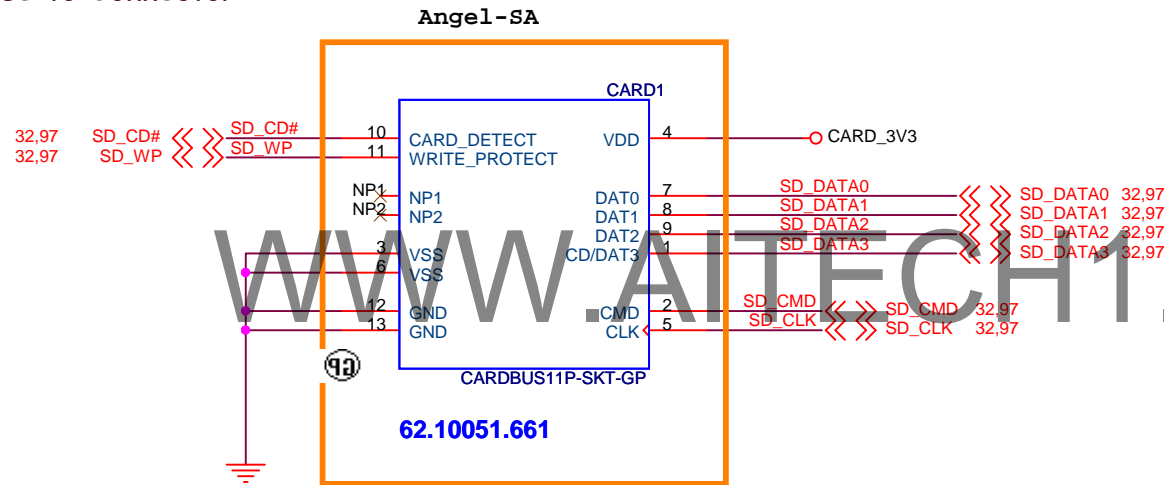
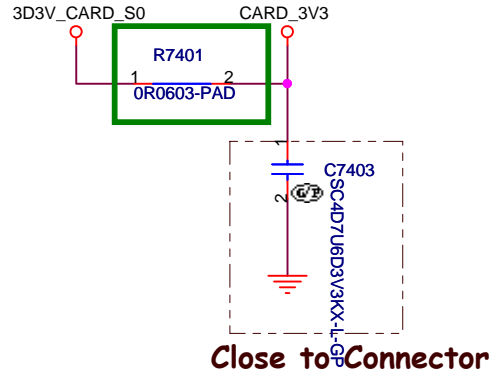
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SD/XD/MS Card Reader



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Title			
CARD Reader CONN			
Size	Document Number		Rev
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SSID = ExpressCard

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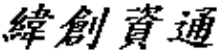
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>New Card</div>		
Size <div>A4</div>	Document Number <div>Angel-CY</div>	Rev <div>1</div>
Date <div>Monday, April 22, 2013</div>		Sheet <div>75</div> of <div>102</div>

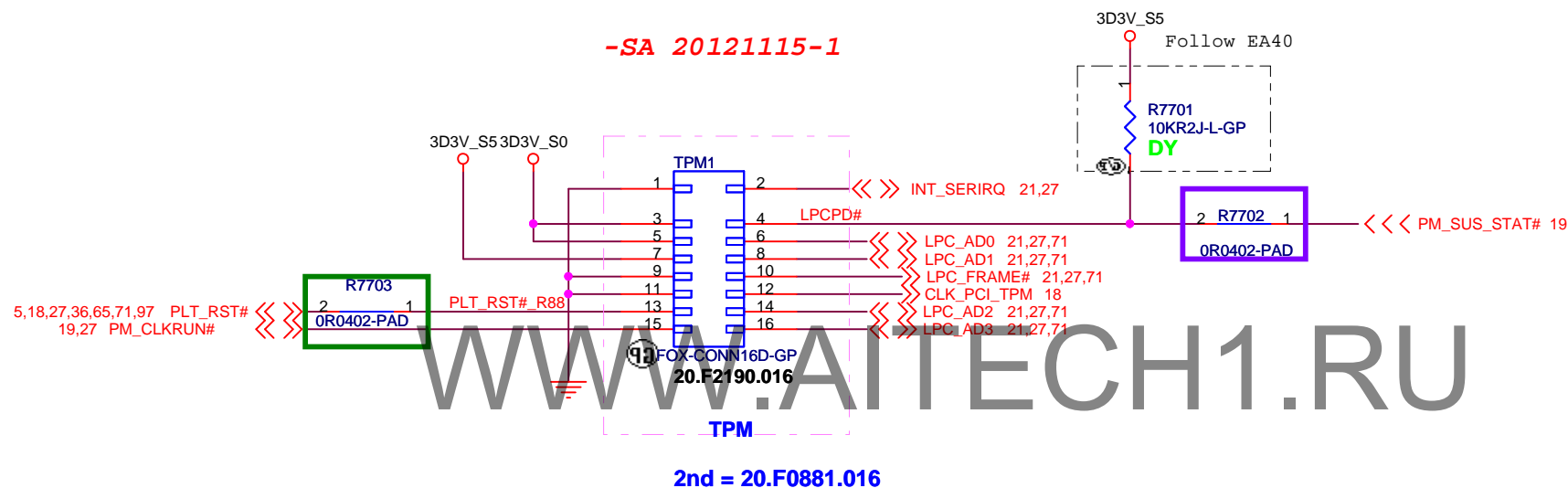
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<Variant Name>

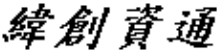
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
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Title Reserved			
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SSID - User Interface

Free Fall Sensor

Note

- no via trace under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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Title			
Free Fall Sensor			
Size A4	Document Number Angel-CY		Rev 1
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Note

- 1) Keep all signals are the same trace width. (included VDD, GND).
- 2) No VIA under IC bottom.

5

4

3

2

1

D

D

C

C

B

B

A

A

Angel-SA

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Title		
Reserved		
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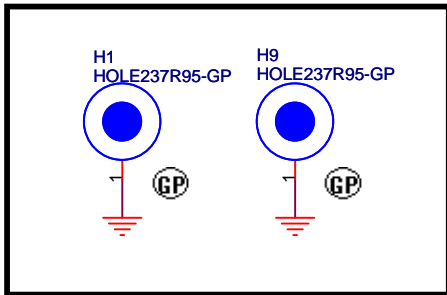
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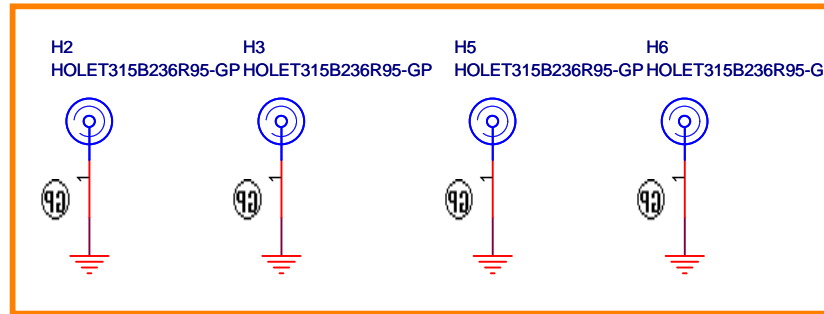
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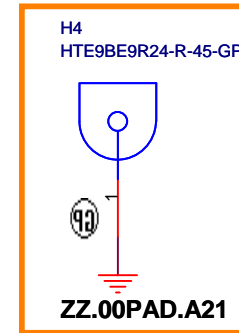
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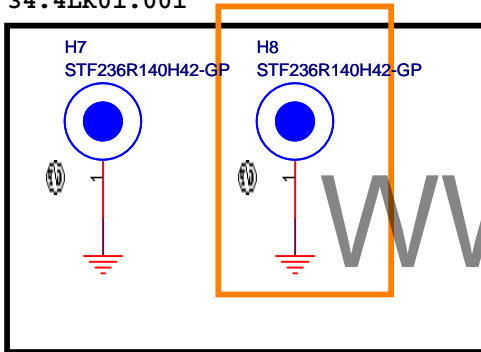


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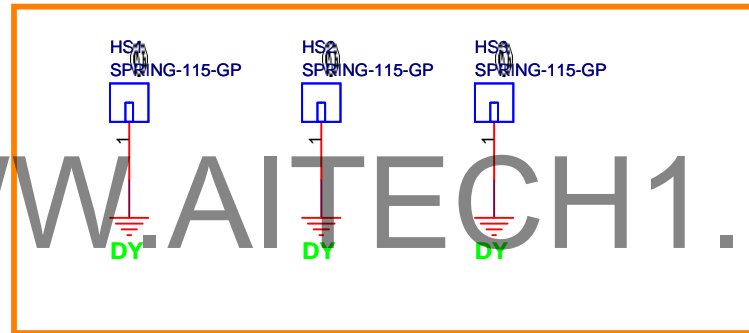
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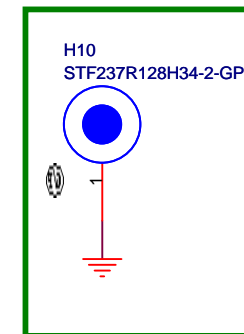


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H10
STF237R128H34-2-GP



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Title

Reserved

Size
A4

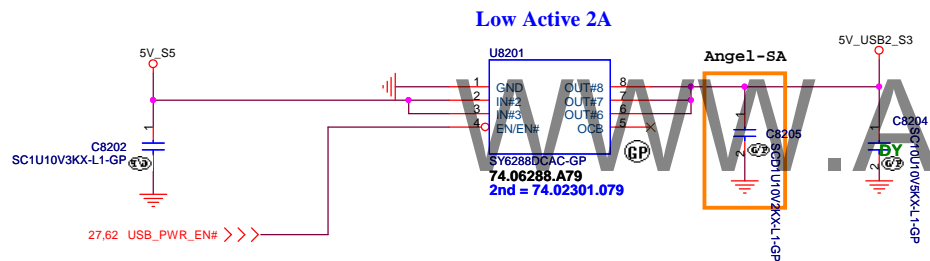
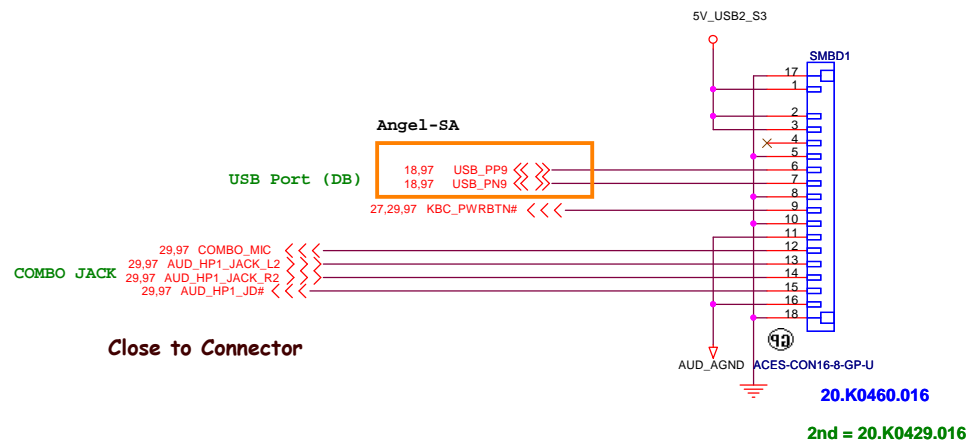
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IO Board Connector			
Size A3	Document Number		Rev 1
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Title GPU(PEG)			
Size A2	Document Number	Rev	1
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Title			
GPU (DIGITALOUT)			
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Title			
GPU (VRAM I/F)			
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GPU (GPIO/STRAP)	
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Title			
GPU (POWER/GND)			
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GPU-VRAM1,2 (1/4)			
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GPU-VRAM3,4 (2/4)			
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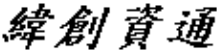
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Title		
GPU-VRAM5,6 (3/4)		
Size	Document Number	Rev
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A2	Angel-CY	1	
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Title			
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Size	Document Number	Rev	
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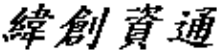
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Size <div>A4</div>	Document Number <div>Angel-CY</div>	Rev <div>1</div>
Date <div>Monday, April 22, 2013</div>		Sheet <div>94</div> of <div>102</div>

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SSID = SDIO

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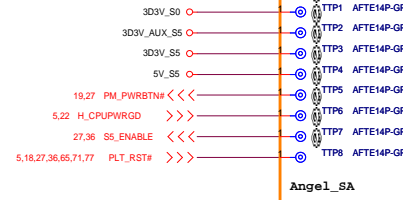
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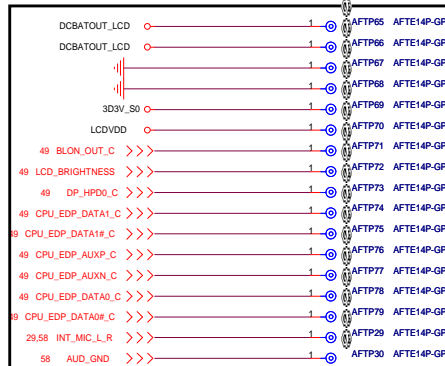
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Size	Document Number	Rev
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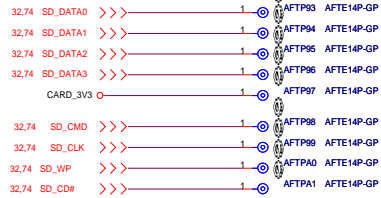
Check test point



Test Point放在Dimm Door打開可量測處



EDP + MIC connector



Card reader connector

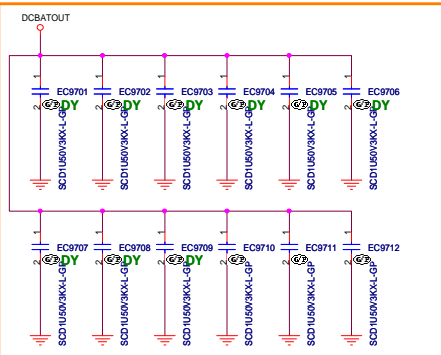


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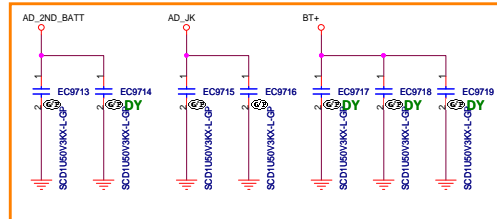


PWR connector

Angel_SA



Angel_SA



Angel_SA

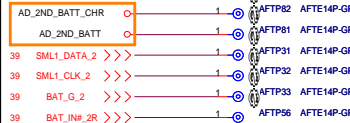


DC IN connector



Battery connector

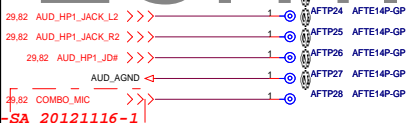
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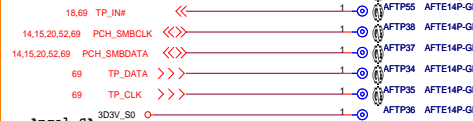
Second Battery connector



Speaker connector



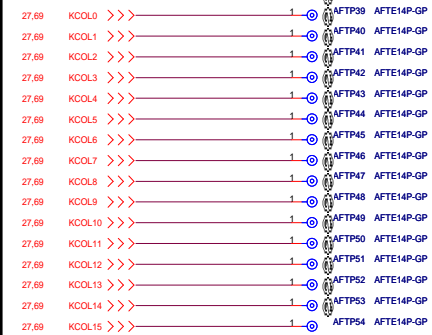
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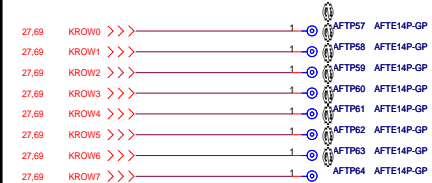
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FAN connector



Normal KB connector



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Title		UNUSED PARTS/EMI Capacitors	
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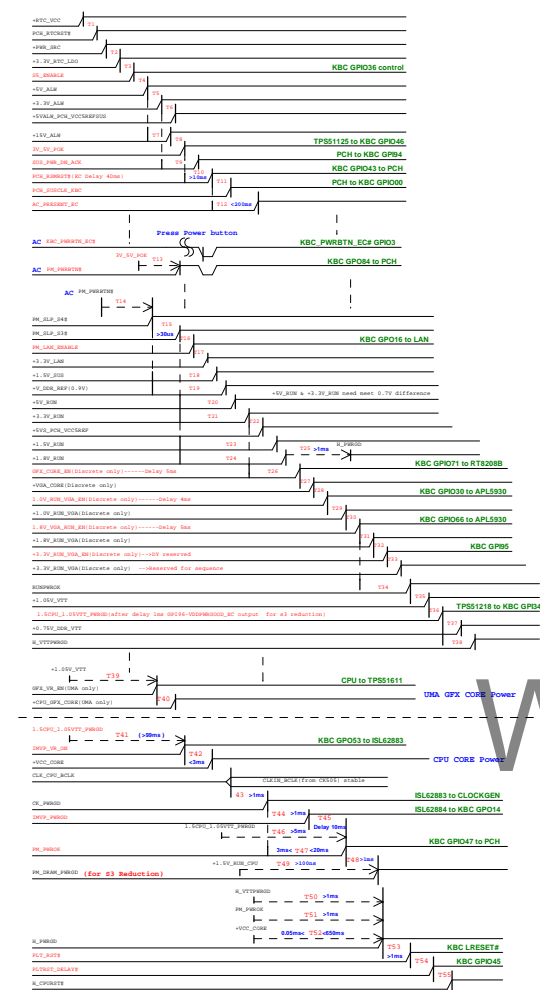
Rev
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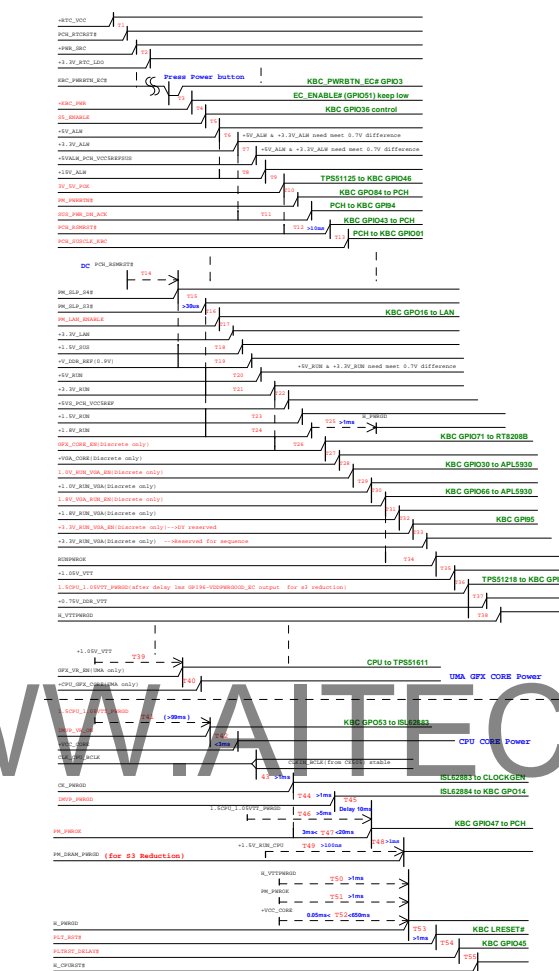
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Intel- Power Up Sequence

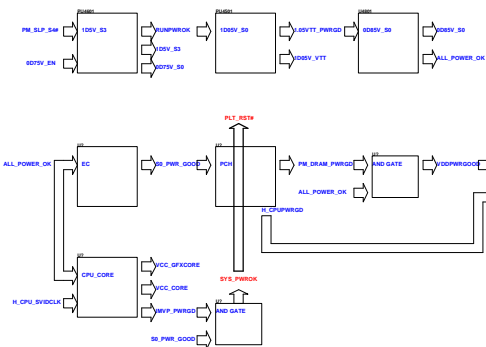
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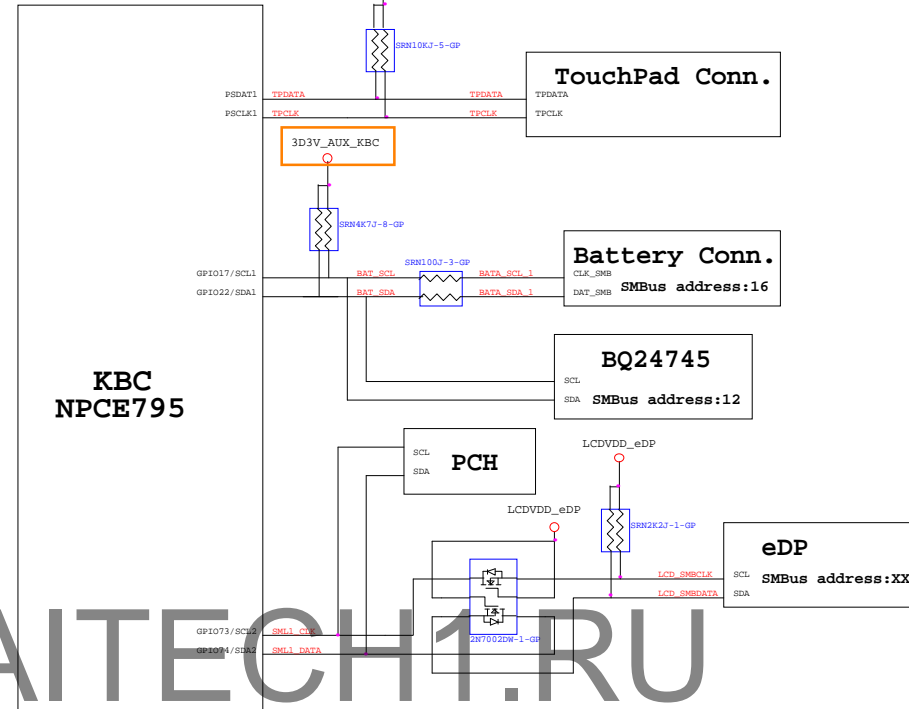
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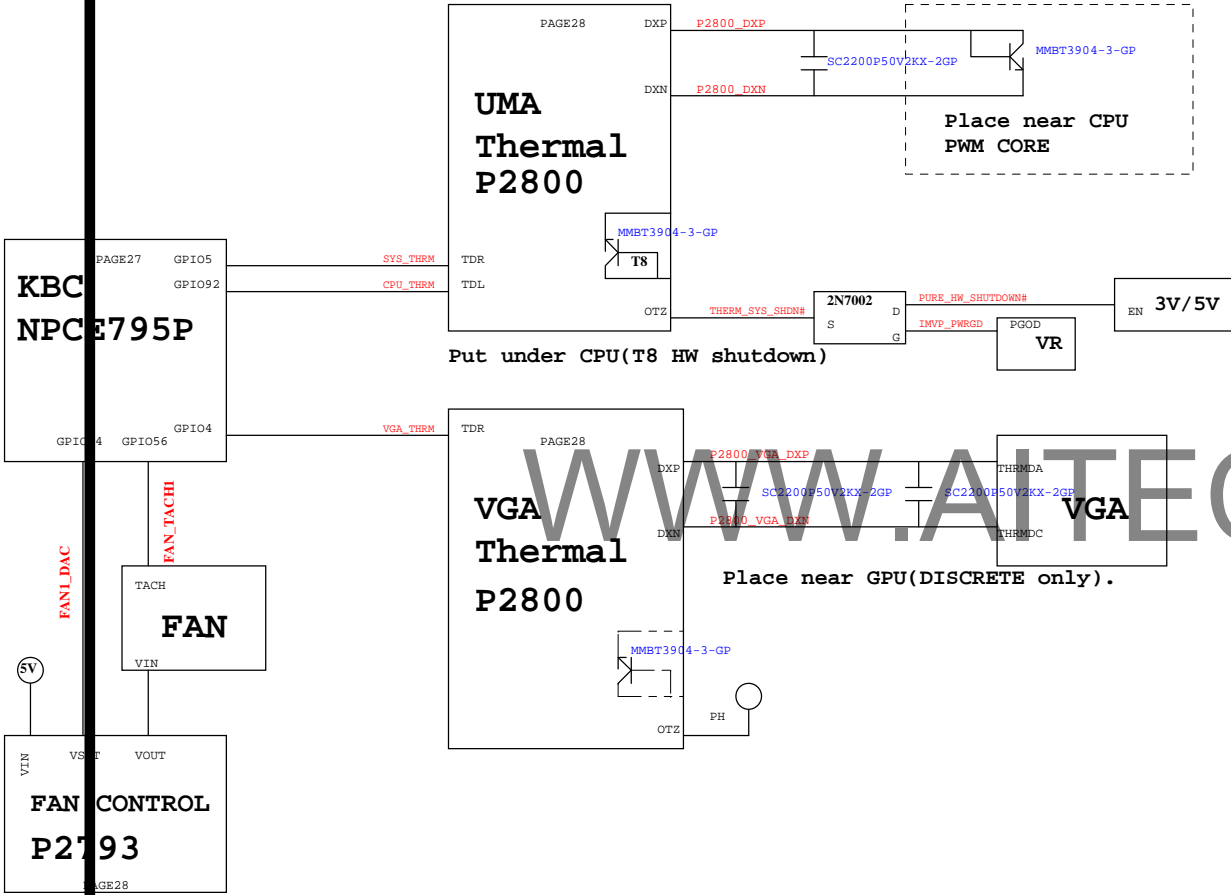
Power Sequence



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

